BLF8G24LS-100V; BLF8G24LS-100GV Power LDMOS transistor Rev. 4 – 1 September 2015

AMPLEON Product data sheet

Product profile 1.

1.1 General description

100 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 2300 MHz to 2400 MHz.

Table 1. **Typical performance**

Typical RF performance at $T_{case} = 25 \ ^{\circ}C$ in a common source class-AB production test circuit.

Test signal	f	l _{Dq}	V _{DS}	P _{L(AV)}	G _p	η _D	ACPR _{5M}
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	2300 to 2400	900	28	25	19	32	–29 <mark>[1]</mark>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; 5 MHz carrier spacing.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth (90 MHz typical)
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range

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2. Pinning information

Table 2.	Pinning		
Pin	Description	Simplified outline	Graphic symbol
BLF8G24	LS-100V (SOT1244B)		
1	drain		
2	gate		6 7 → 1 → 4,5
3	source [1]		
4	decoupling lead	3	2
5	decoupling lead		aaa-003619
6	n.c.		
7	n.c.	6 2 7	
BLF8G24	LS-100GV (SOT1244C)		
1	drain		
2	gate		6 7 → 1 → 4,5
3	source [1]		
4	decoupling lead		2
5	decoupling lead		aaa-003619
6	n.c.	6 2 7 3	
7	n.c.		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package					
	Name	Description	Version				
BLF8G24LS-100V	-	earless flanged ceramic package; 6 leads	SOT1244B				
BLF8G24LS-100GV	-	earless flanged ceramic package; 6 leads	SOT1244C				

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	65	V
V _{GS}	gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5.	Thermal characteristics			
Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T _{case} = 80 °C; P _L = 48 W	0.29	K/W

6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 1 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 153 mA	1.5	1.9	2.3	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 900 mA	1.6	2	2.4	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	4.2	μA
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	29	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	420	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 153 mA	-	1.27	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ I _D = 5.35 A	-	0.1	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on the CCDF; $f_1 = 2302.5$ MHz; $f_2 = 2307.5$ MHz; $f_3 = 2392.5$ MHz; $f_4 = 2397.5$ MHz; RF performance at $V_{DS} = 28$ V; $I_{Dq} = 900$ mA; $T_{case} = 25$ °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G _p	power gain	P _{L(AV)} = 25 W	18	19	-	dB
η _D	drain efficiency	P _{L(AV)} = 25 W	29	32	-	%
RL _{in}	input return loss	P _{L(AV)} = 25 W	-	-17	-7	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	P _{L(AV)} = 25 W	-	-29	-25	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G24LS-100V and BLF8G24LS-100GV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 900 mA; P_L = 100 W; f = 2300 MHz.

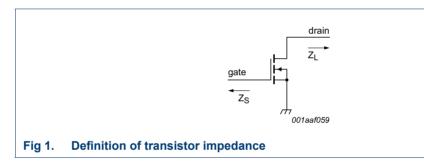
7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data; $I_{Dq} = 900 \text{ mA}$; $V_{DS} = 28 \text{ V}$.

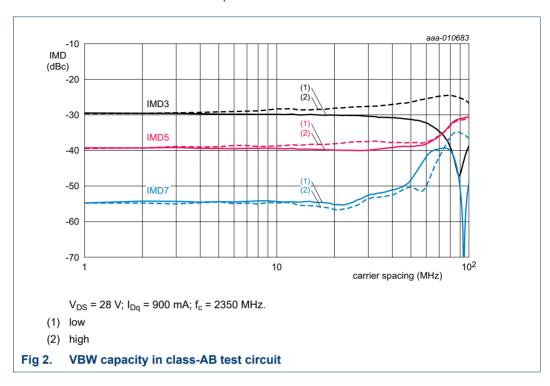
f	Z _S [1]	Z _L [1]
(MHz)	(Ω)	(Ω)
BLF8G24LS-100V		
2300	1.52 – j4.32	1.96 – j2.21
2400	2.54 – j5.05	1.83 – j2.03
2500	4.83 – j5.28	1.76 – j2.23
BLF8G24LS-100GV		
2300	1.60 – j5.88	1.96 – j4.12
2400	2.53 – j6.66	1.81 – j4.12
2500	4.53 – j7.28	1.74 – j4.33

[1] Z_S and Z_L defined in Figure 1.



7.3 VBW in a class-AB operation

The BLF8G24LS-100V and BLF8G24LS-100GV show 90 MHz (typical) video bandwidth (IMD third-order intermodulation inflection point) in a class-AB test circuit in the 2.3 GHz to 2.4 GHz band at V_{DS} = 28 V and I_{Dg} = 0.9 A.



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7.4 Test circuit

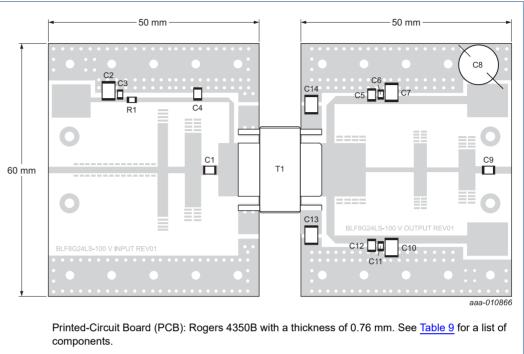


Fig 3. Component layout

Table 9. List of components

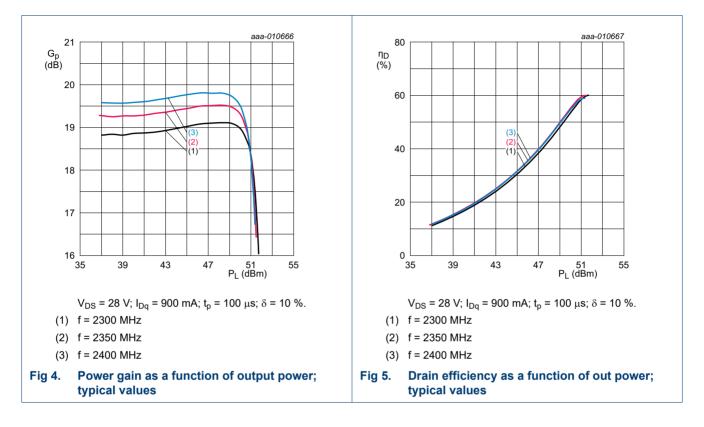
Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	1.0 pF	[1]	ATC 800B
C2	multilayer ceramic chip capacitor	1 μF	[2]	Murata
C3	multilayer ceramic chip capacitor	100 nF	[2]	Murata
C4, C5, C9, C12	multilayer ceramic chip capacitor	24 pF	[1]	ATC 800B
C6, C11	multilayer ceramic chip capacitor	220 nF	[2]	Murata
C7, C10, C13, C14	multilayer ceramic chip capacitor	4.7 μF, 50 V	[2]	Murata
C8	electrolytic capacitor	> 470 μF, 63 V		
R1	chip resistor	4.7 Ω, 1 % tolerance		SMD 0805
T1	transistor	-		Ampleon BLF8G24LS-100V

[1] American Technical Ceramics type 800B or capacitor of same quality.

[2] Murata or capacitor of same quality.

7.5 Graphical data

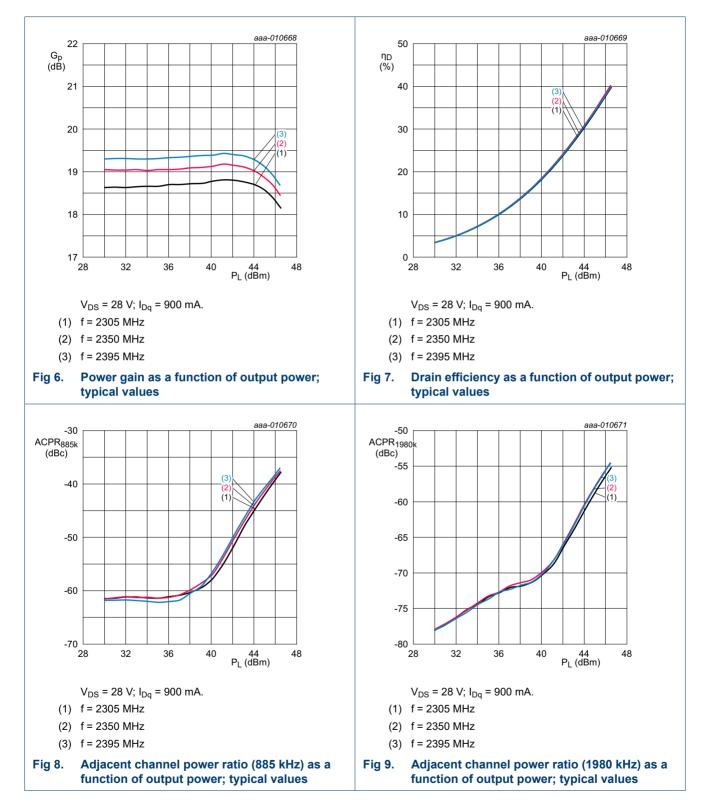
7.5.1 Pulsed CW



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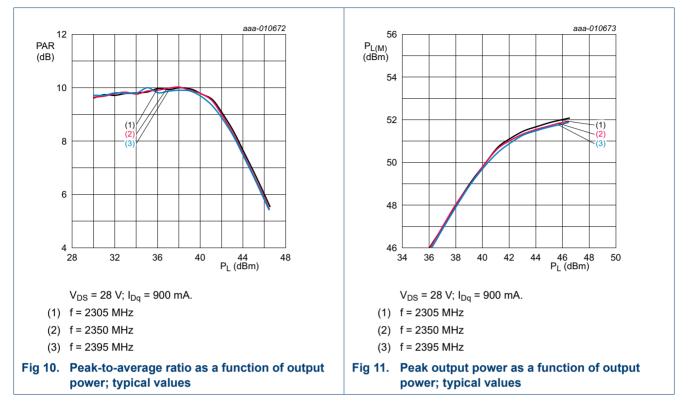
7.5.2 IS-95



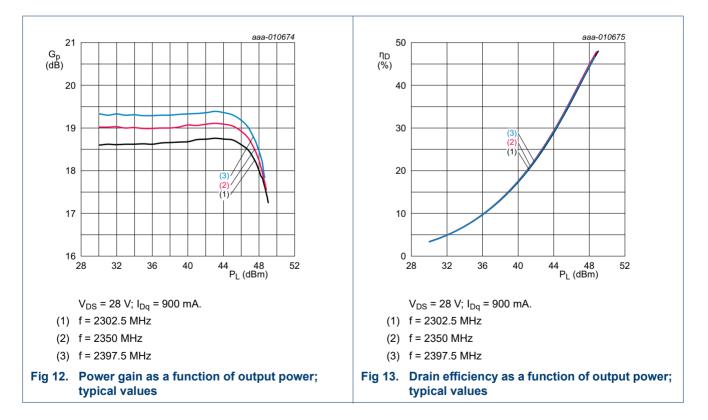
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BLF8G24LS-100(G)V

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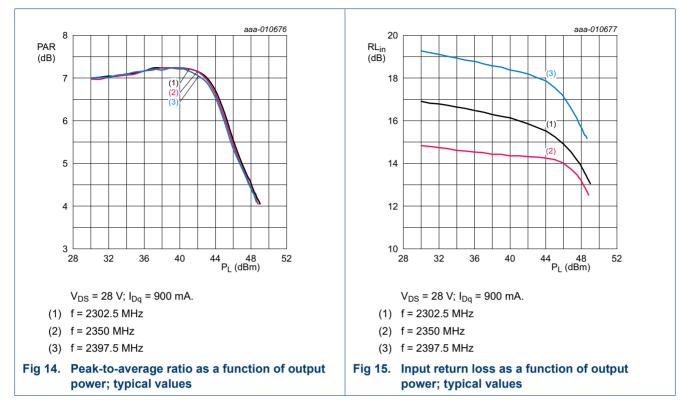


7.5.3 1-Carrier W-CDMA

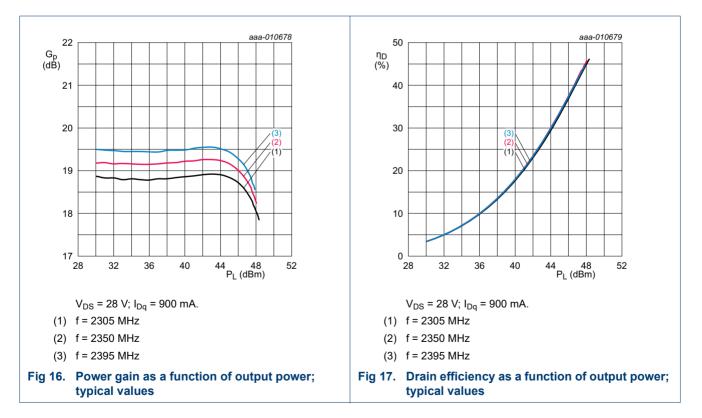


BLF8G24LS-100(G)V

Power LDMOS transistor



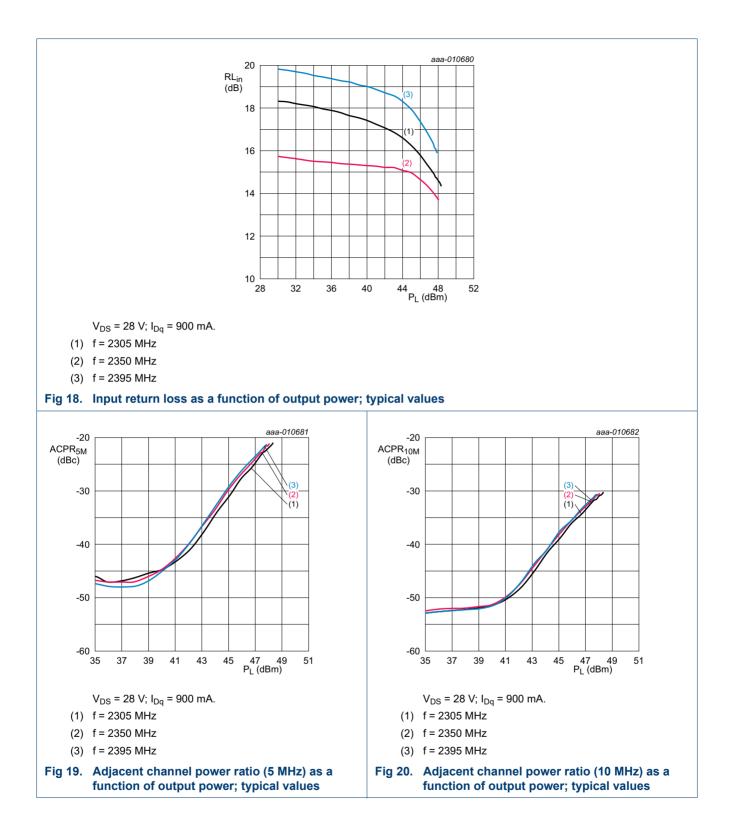
7.5.4 2-Carrier W-CDMA



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8. Package outline

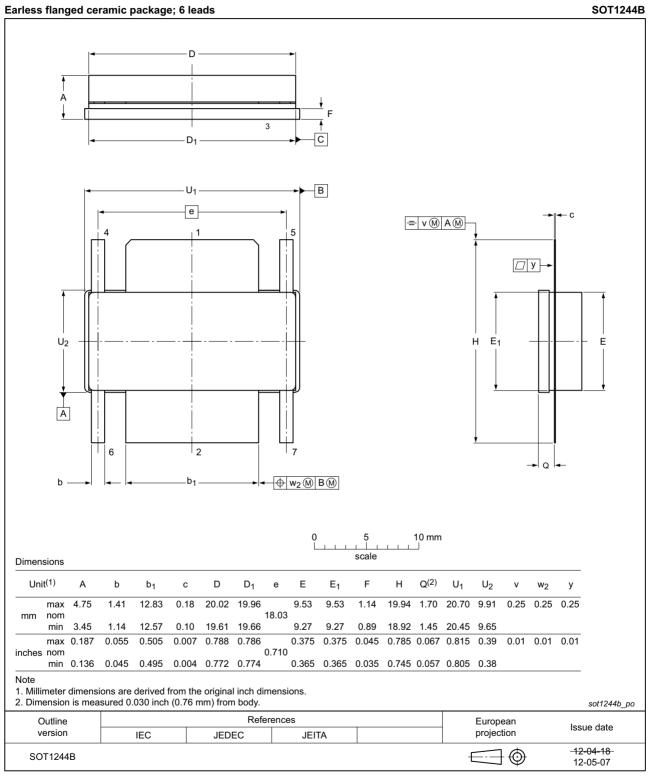


Fig 21. Package outline SOT1244B

BLF8G24LS-100V_24LS-100GV#4

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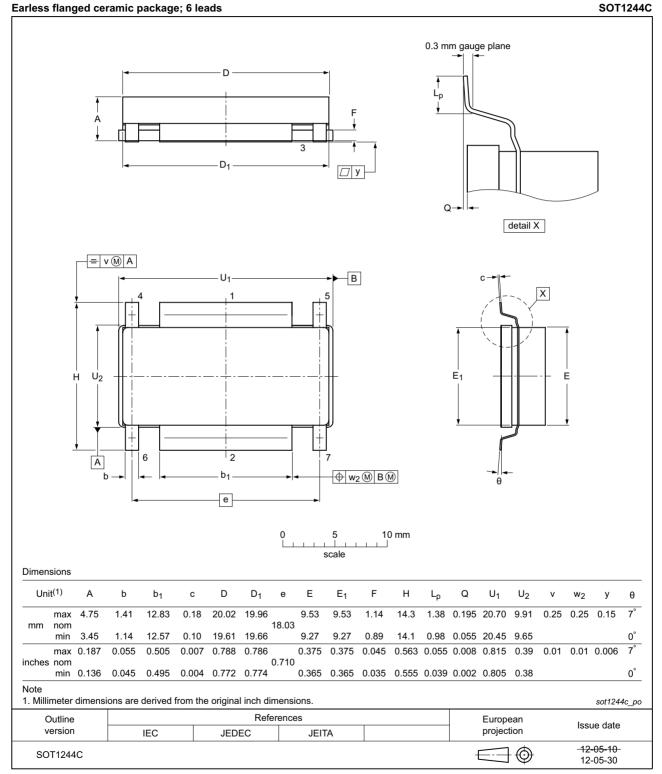


Fig 22. Package outline SOT1244C

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10. Abbre	Table 10. Abbreviations				
Acronym	Description				
3GPP	3rd Generation Partnership Project				
CCDF	Complementary Cumulative Distribution Function				
CW	Continuous Wave				
DPCH	Dedicated Physical CHannel				
ESD	ElectroStatic Discharge				
IS-95	Interim Standard 95				
LDMOS	Laterally Diffused Metal Oxide Semiconductor				
MTF	Median Time to Failure				
PAR	Peak-to-Average Ratio				
SMD	Surface Mounted Device				
VBW	Video BandWidth				
VSWR	Voltage Standing Wave Ratio				
W-CDMA	Wideband Code Division Multiple Access				

11. Revision history

Table 11. Revision history							
Document ID	Release date	Data sheet status	Change notice	Supersedes			
BLF8G24LS-100V_24LS-100GV#4	20150901	Product data sheet		BLF8G24LS-100V_ 24LS-100GV v.3			
Modifications:	identity guid	of this document has beer delines of Ampleon. have been adapted to the	C C				
BLF8G24LS-100V_24LS-100GV v.3	20140627	Product data sheet	-	BLF8G24LS-100V_ 24LS-100GV v.2			
BLF8G24LS-100V_24LS-100GV v.2	20140228	Objective data sheet	-	BLF8G24LS-100V_ 24LS-100GV v.1			
BLF8G24LS-100V_24LS-100GV v.1	20131104	Objective data sheet	-	-			

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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