

# BLC8G20LS-400AV

Power LDMOS transistor

Rev. 4 — 24 November 2017

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty production test circuit.

$V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 800\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.4\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	32	85	15.5	44	-31 [1]
	1930 to 1990	32	85	15.5	44	-35 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01% probability on CCDF.

### 1.2 Features and benefits

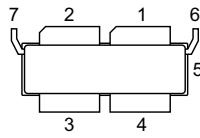
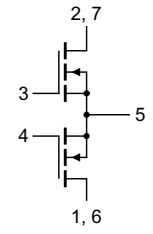
- Excellent ruggedness
- Excellent electrical stability
- Suitable for conventional and inverted Doherty
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		 <p>aaa-014884</p>
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source <a href="#">[1]</a>		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC8G20LS-400AV	-	Air cavity plastic earless flanged package; 6 leads	SOT1258-1

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{case}$	case temperature		-40	+125	°C

## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA (main)};$ $V_{GS(amp)peak} = 0.4\text{ V}; T_{case} = 80\text{ }^{\circ}\text{C}.$		
		$P_L = 85\text{ W}$	0.32	K/W
		$P_L = 110\text{ W}$	0.31	K/W

## 7. Characteristics

Table 7. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.8\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 180\text{ mA}$	1.5	1.9	2.3	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 32\text{ V}; I_D = 800\text{ mA}$	1.7	2.1	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	34	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 9.0\text{ A}$	-	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 6.3\text{ A}$	-	85	135	m $\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3.0\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 300\text{ mA}$	1.5	1.9	2.3	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 32\text{ V}; I_D = 1800\text{ mA}$	1.7	2.1	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	50	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 15.0\text{ A}$	-	19	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 10.5\text{ A}$	-	55	85	m $\Omega$

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH;  $f_1 = 1807.5\text{ MHz}; f_2 = 1877.5\text{ MHz};$  RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA (main)};$   $V_{GS(amp)peak} = 0.4\text{ V}; T_{case} = 25\text{ }^{\circ}\text{C};$  unless otherwise specified; in an asymmetrical Doherty production test circuit in 1805 MHz to 1880 MHz frequency range.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 85\text{ W}$	14.5	15.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 85\text{ W}$	-	-11	-7	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 85\text{ W}$	40	44	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 85\text{ W}$	-	-31	-27	dBc
PAR <sub>O</sub>	output peak-to-average ratio	$P_{L(AV)} = 100\text{ W}$	6.0	6.7	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)} = 100\text{ W}$	400	475	-	W

## 8. Test information

### 8.1 Ruggedness in Doherty operation

The BLC8G20LS-400AV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:

- $V_{DS} = 28\text{ V}$ ;  $I_{DQ} = 800\text{ mA}$ ;  $V_{GS(amp)peak} = 0.4\text{ V}$ ;  $f = 1807.5\text{ MHz}$ :  
1-carrier W-CDMA;  $P_L = 141\text{ W}$  (5 dB OBO); 100 % clipping
- $V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 800\text{ mA}$ ;  $V_{GS(amp)peak} = 0.4\text{ V}$ ;  $f = 1807.5\text{ MHz}$ :  
1-carrier W-CDMA;  $P_L = 141\text{ W}$  (5 dB OBO); 100 % clipping

### 8.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{DQ} = 800\text{ mA}$  (main);  $V_{DS} = 32\text{ V}$ ; pulsed CW ( $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ).

f (MHz)	Z <sub>S</sub> [1] ( $\Omega$ )	Z <sub>L</sub> [1] ( $\Omega$ )	P <sub>L</sub> [2] (W)	$\eta_D$ [2] (%)	G <sub>p</sub> [2] (dB)
<b>Maximum power load</b>					
1805	1.2 – j5.2	1.3 – j4.4	252	55.9	18.0
1840	1.2 – j5.3	1.2 – j4.5	249	55.6	18.1
1880	1.6 – j5.9	1.2 – j4.4	245	53.1	17.9
<b>Maximum drain efficiency load</b>					
1805	1.2 – j5.2	2.5 – j4.0	178	61.4	20.0
1840	1.2 – j5.3	2.5 – j4.1	182	61.4	20.2
1880	1.6 – j5.9	2.6 – j3.9	176	60.8	20.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.

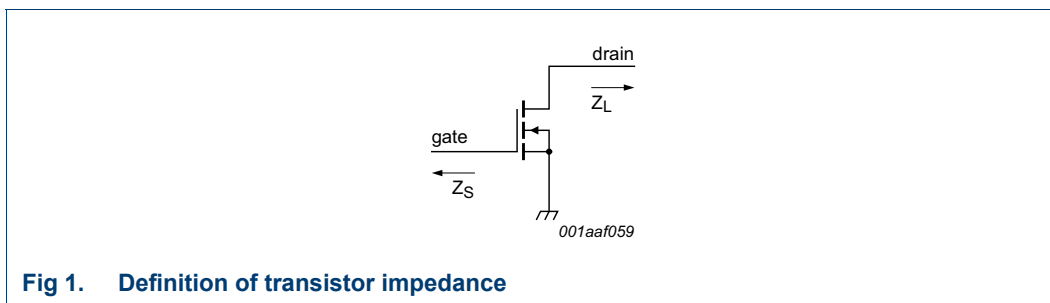
**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{DQ} = 1750\text{ mA}$  (peak);  $V_{DS} = 32\text{ V}$ ; pulsed CW ( $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ).

f (MHz)	Z <sub>S</sub> [1] ( $\Omega$ )	Z <sub>L</sub> [1] ( $\Omega$ )	P <sub>L</sub> [2] (W)	$\eta_D$ [2] (%)	G <sub>p</sub> [2] (dB)
<b>Maximum power load</b>					
1805	1.2 – j5.0	2.1 – j5.4	394	50.8	19.0
1840	1.5 – j5.3	2.5 – j5.3	383	53.5	19.5
1880	2.0 – j5.9	2.3 – j5.5	378	52.1	19.4
<b>Maximum drain efficiency load</b>					
1805	1.2 – j5.0	2.5 – j3.8	289	57.8	21.4
1840	1.5 – j5.3	2.7 – j3.7	289	59.4	21.4
1880	2.0 – j5.9	2.4 – j3.8	284	60.4	21.7

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] At 3 dB gain compression.



### 8.3 Recommended impedances for Doherty design

**Table 11. Typical impedance of main at 1 : 1 load**

Measured load-pull data of main device;  $I_{Dq} = 800 \text{ mA}$  (main);  $V_{DS} = 32 \text{ V}$ ; pulsed CW ( $t_p = 100 \text{ }\mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	$Z_S$ [1] ( $\Omega$ )	$Z_L$ [1] ( $\Omega$ )	$P_{L(3dB)}$ [2] (W)	$\eta_D$ [2] (%)	$G_p$ [2] (dB)
1805	1.0 – j4.8	1.8 – j4.9	179	50.4	18.1
1840	1.1 – j5.0	1.7 – j4.6	189	51.6	18.3
1880	1.4 – j5.2	1.7 – j4.3	183	49.3	18.5

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

[2] At  $P_{L(AV)} = 85 \text{ W}$ .

**Table 12. Typical impedance of main device at 1 : 2.5 load**

Measured load-pull data of main device;  $I_{Dq} = 800 \text{ mA}$  (main);  $V_{DS} = 32 \text{ V}$ ; pulsed CW ( $t_p = 100 \text{ }\mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	$Z_S$ [1] ( $\Omega$ )	$Z_L$ [1] ( $\Omega$ )	$P_{L(3dB)}$ [2] (W)	$\eta_D$ [2] (%)	$G_p$ [2] (dB)
1805	1.0 – j4.8	3.1 – j3.5	132	51.1	19.7
1840	1.1 – j5.0	3.3 – j4.0	126	50.5	19.9
1880	1.4 – j5.2	3.3 – j4.2	126	50.7	19.9

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

[2] At  $P_{L(AV)} = 85 \text{ W}$ .

**Table 13. Typical impedance of peak device at 1 : 1 load**

Measured load-pull data of peak device;  $I_{Dq} = 1750 \text{ mA}$  (peak);  $V_{DS} = 32 \text{ V}$ ; pulsed CW ( $t_p = 100 \text{ }\mu\text{s}$ ;  $\delta = 10 \%$ ).

f (MHz)	$Z_S$ [1] ( $\Omega$ )	$Z_L$ [1] ( $\Omega$ )	$P_{L(3dB)}$ [2] (W)	$\eta_D$ [2] (%)	$G_p$ [2] (dB)
1805	1.2 – j5.0	2.8 – j4.8	316	50.0	19.0
1840	1.5 – j5.3	2.7 – j4.6	313	51.4	19.4
1880	2.0 – j5.9	2.6 – j4.3	290	52.9	20.0

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

[2] At  $P_{L(AV)} = 85 \text{ W}$ .

Table 14. Off-state impedances of peak device

f (MHz)	Z <sub>off</sub> (Ω)
1805	0.9 – j0.2
1840	0.9 – j0.1
1880	0.9 – j0.2

8.4 Test circuit

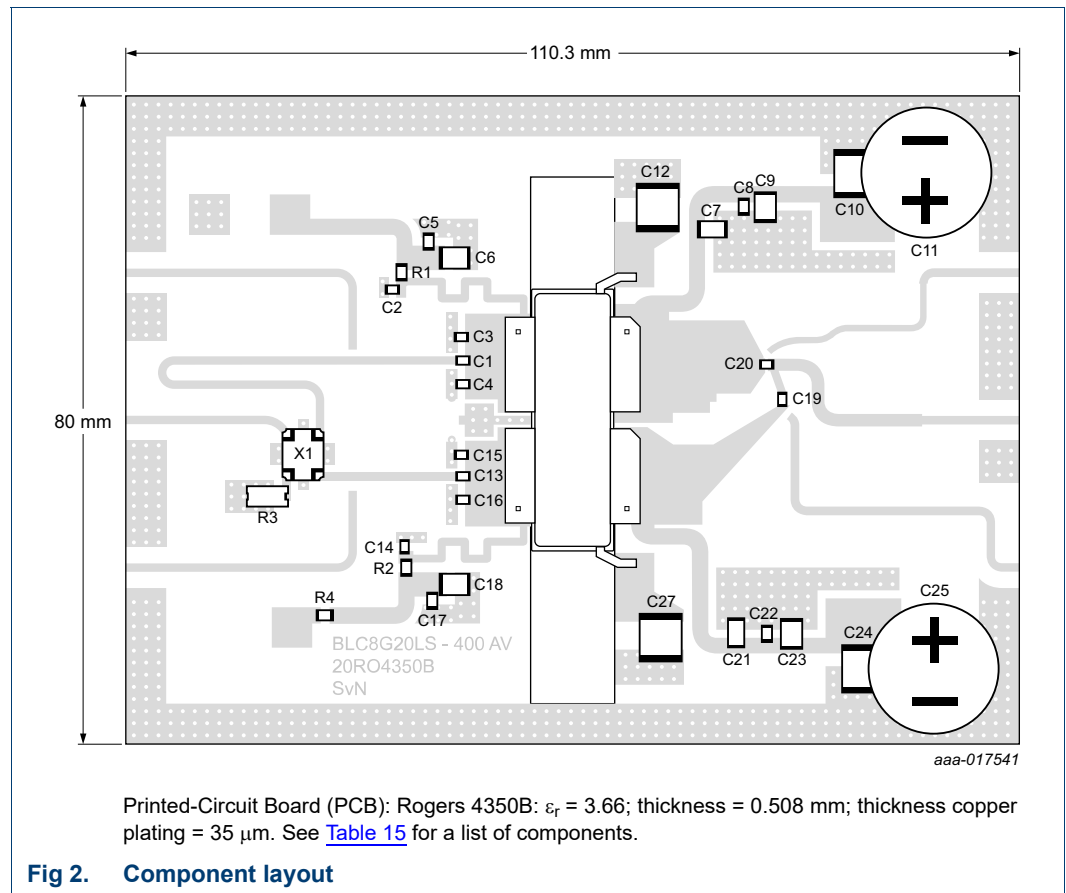


Table 15. List of components

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C2, C13, C14, C19	multilayer ceramic chip capacitor	10 pF	[1] ATC 100A
C3, C15	multilayer ceramic chip capacitor	2.2 pF	[1] ATC 100A
C4, C16	multilayer ceramic chip capacitor	2.0 pF	[1] ATC 100A
C5, C8, C17, C22	multilayer ceramic chip capacitor	100 nF	[2] Murata
C6, C9, C18, C23	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$	[2] Murata
C7, C21	multilayer ceramic chip capacitor	10 pF	[3] ATC 100B
C10, C24	multilayer ceramic chip capacitor	10 $\mu\text{F}$ , 50 V	TDK C5750X7

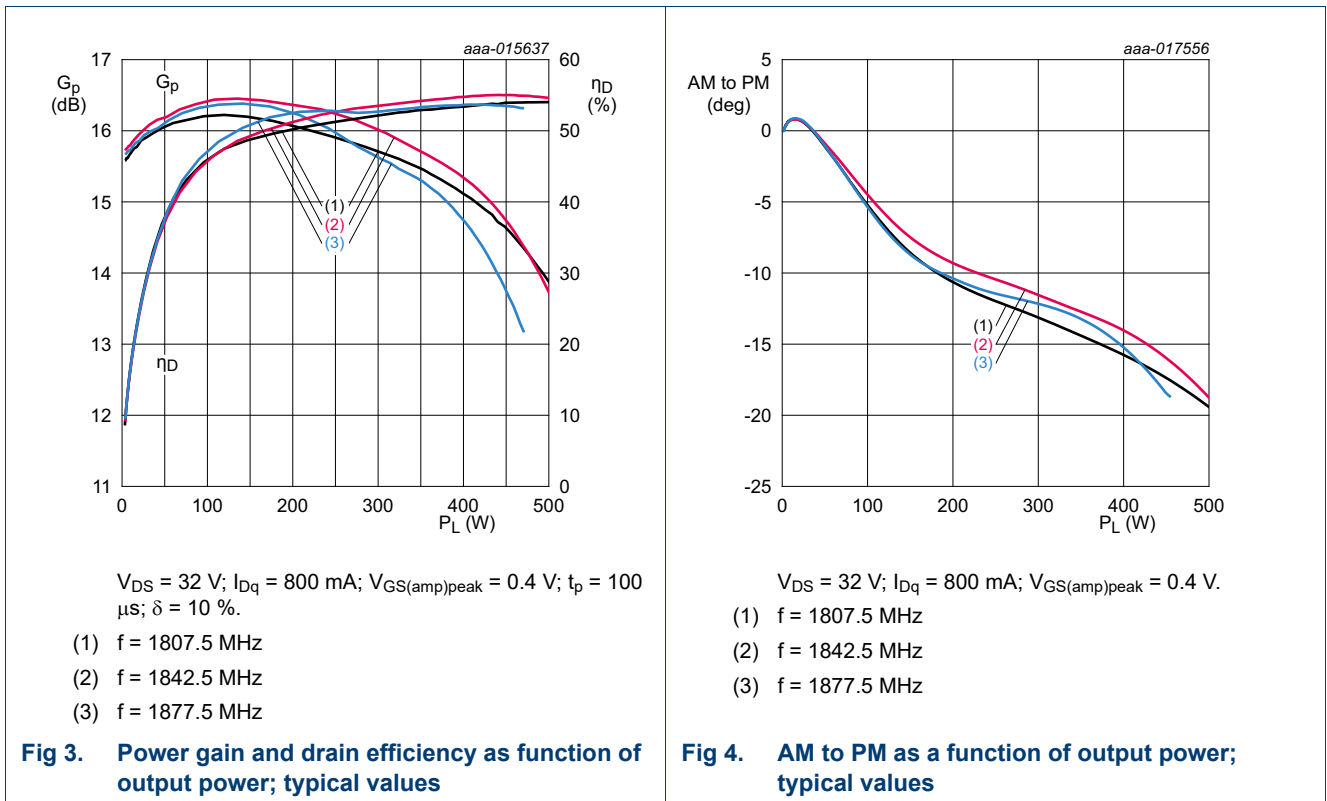
**Table 15. List of components ...continued**  
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C11; C25	electrolytic capacitor	470 $\mu$ F, 63 V	Vishay 148RUS
C12; C26	multilayer ceramic chip capacitor	4.7 $\mu$ F, 100 V	TDK C5750X7
C20	multilayer ceramic chip capacitor	5.6 pF	
R1, R2	SMD resistor	4.7 $\Omega$	SMD 0805
R3	SMD resistor	50 $\Omega$	SMD 0805
R4	SMD resistor	470 $\Omega$	SMD 0805
X1	directional coupler	5 dB	Anaren X3C19P1-05S

- [1] American Technical Ceramics type 100A or capacitor of same quality.
- [2] Murata or capacitor of same quality.
- [3] American Technical Ceramics type 100B or capacitor of same quality.

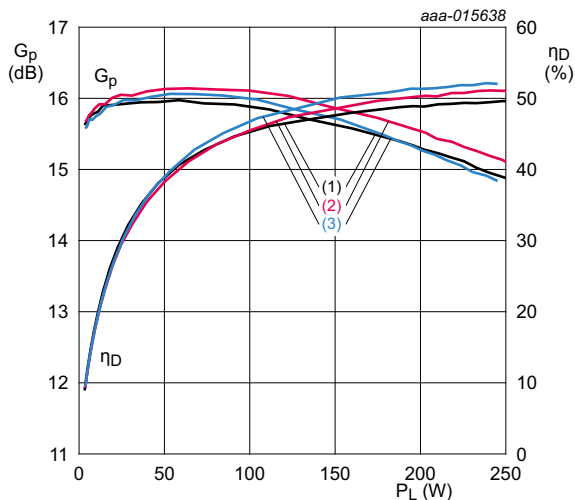
## 8.5 Graphical data

### 8.5.1 Pulsed CW



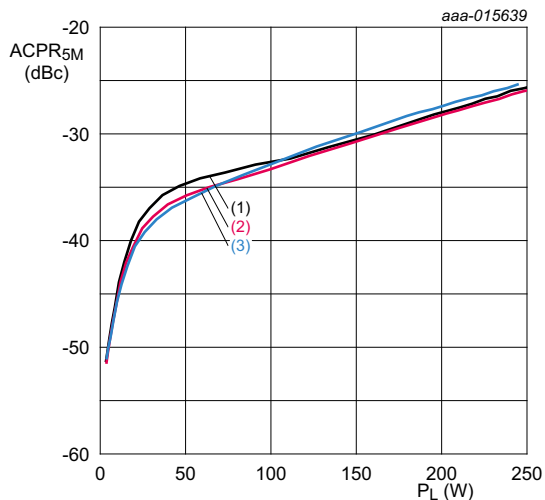
8.5.2 1-Carrier W-CDMA

PAR = 9.6 dB per carrier at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



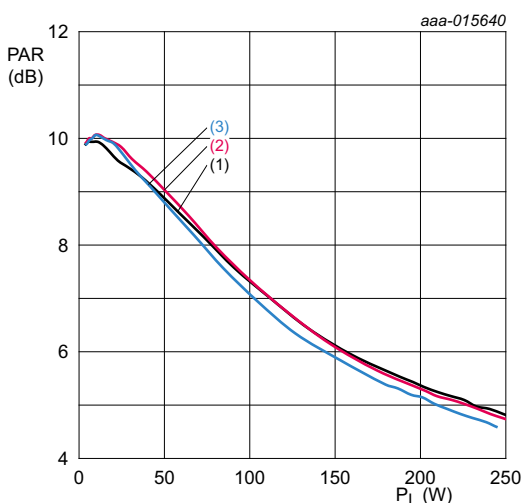
$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$   
 (1)  $f = 1807.5\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1877.5\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



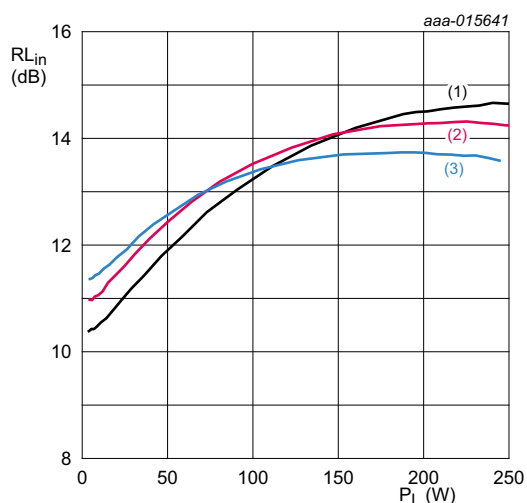
$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$   
 (1)  $f = 1807.5\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1877.5\text{ MHz}$

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$   
 (1)  $f = 1807.5\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1877.5\text{ MHz}$

Fig 7. Peak-to-average power ratio as a function of output power; typical values



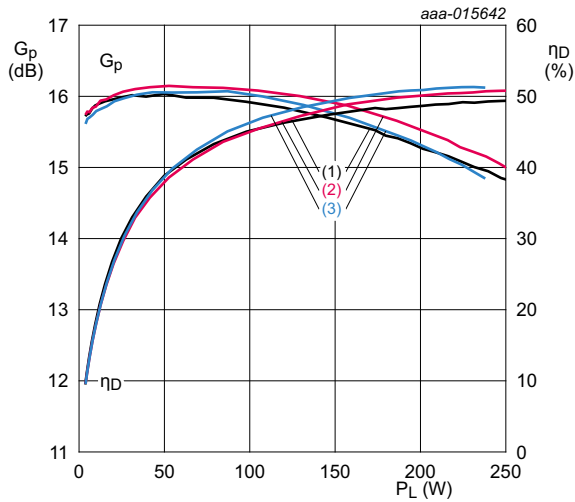
$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$   
 (1)  $f = 1807.5\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1877.5\text{ MHz}$

Fig 8. Input return loss as a function of output power; typical values



8.5.3 2-Carrier W-CDMA

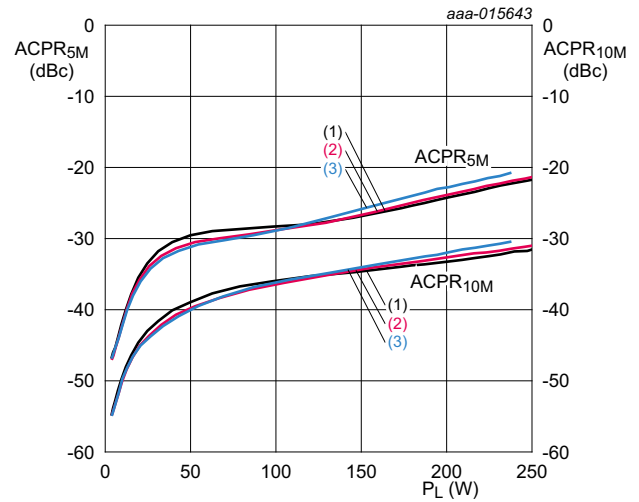
PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (46 % clipping).



$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$

- (1)  $f = 1807.5\text{ MHz}$
- (2)  $f = 1842.5\text{ MHz}$
- (3)  $f = 1877.5\text{ MHz}$

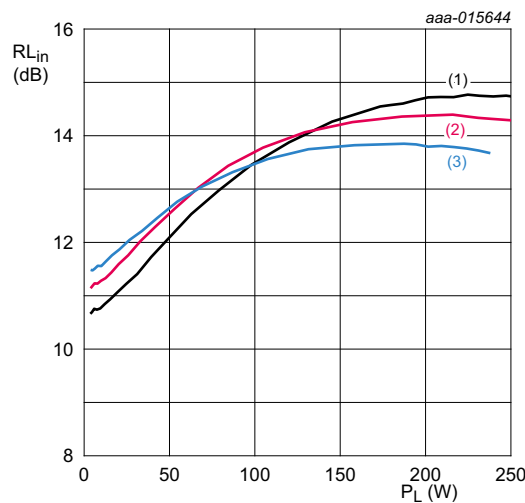
Fig 9. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$

- (1)  $f = 1807.5\text{ MHz}$
- (2)  $f = 1842.5\text{ MHz}$
- (3)  $f = 1877.5\text{ MHz}$

Fig 10. Adjacent channel power ratio (5 MHz) and adjacent channel power ratio (10 MHz) as function of output power; typical values

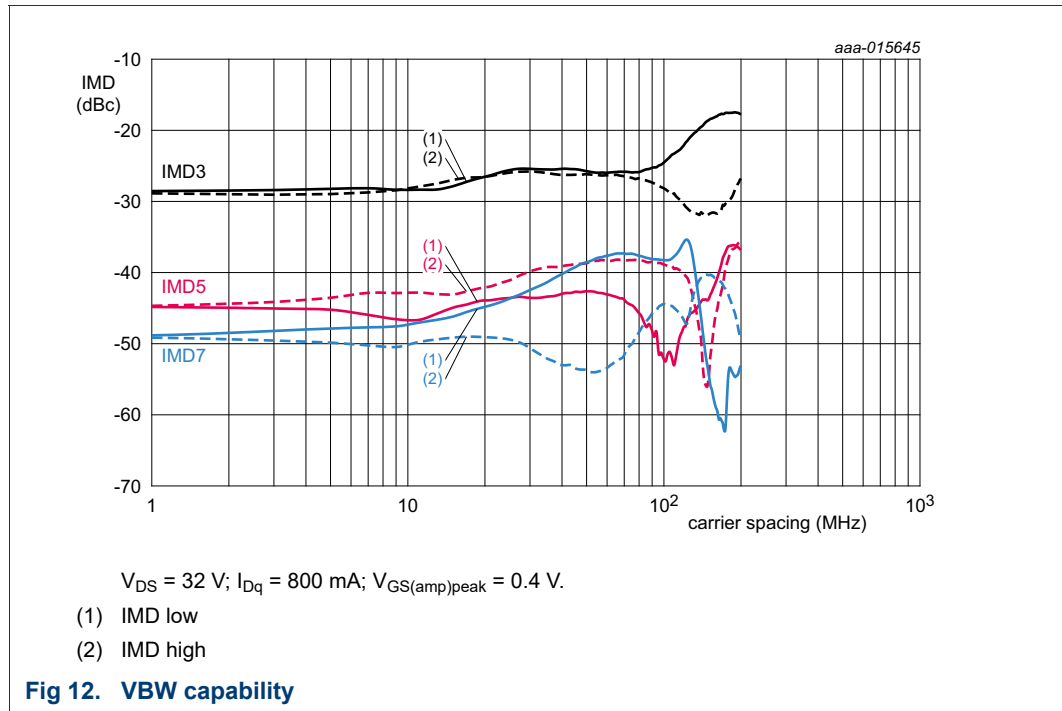


$V_{DS} = 32\text{ V}; I_{Dq} = 800\text{ mA}; V_{GS(amp)peak} = 0.4\text{ V}.$

- (1)  $f = 1807.5\text{ MHz}$
- (2)  $f = 1842.5\text{ MHz}$
- (3)  $f = 1877.5\text{ MHz}$

Fig 11. Input return loss as a function of output power; typical values

8.5.4 2-Tone VBW



9. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-1

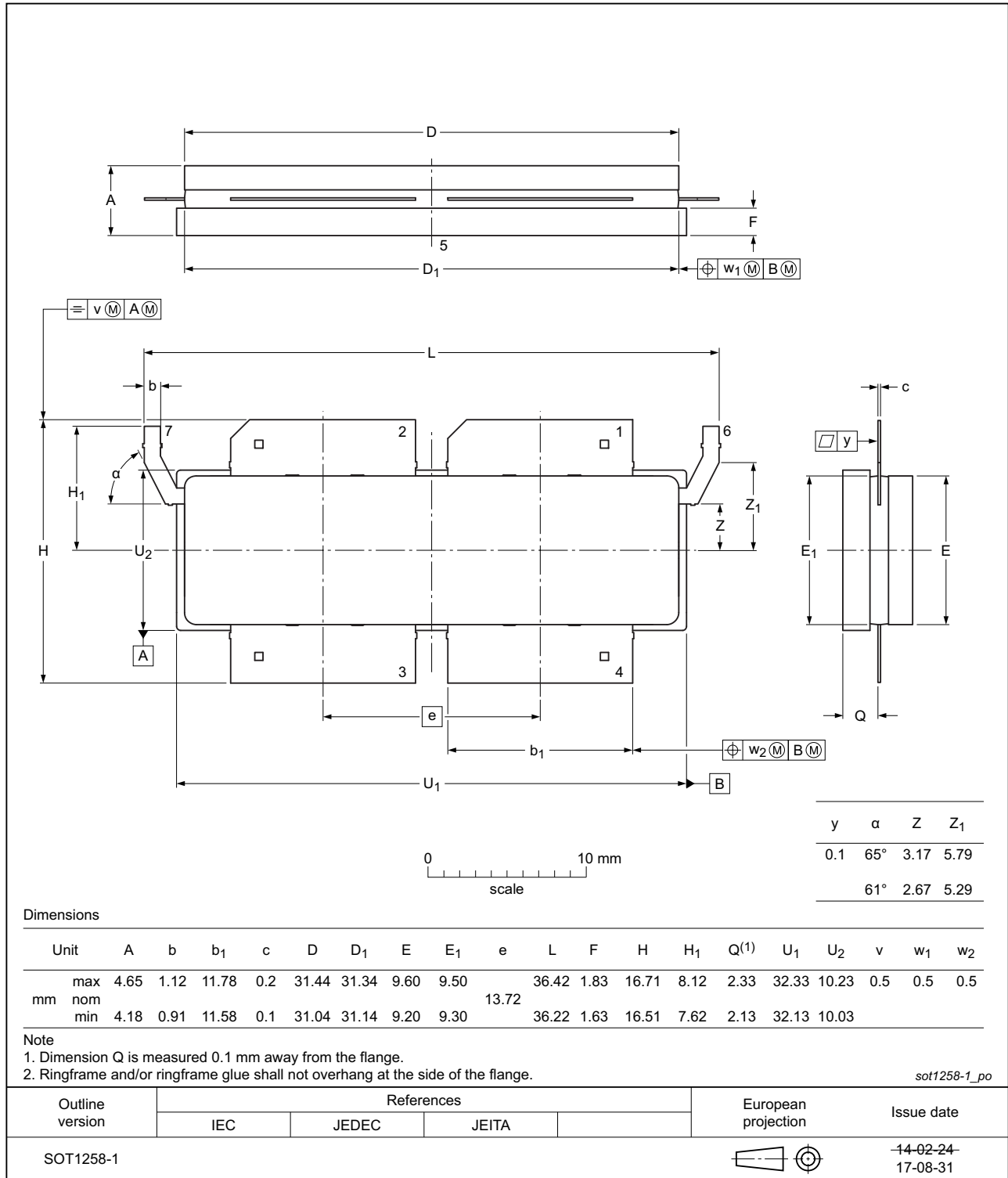


Fig 13. Package outline SOT1258-1

## 10. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 16. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 11. Abbreviations

**Table 17. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 12. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC8G20LS-400AV v.4	20171124	Product data sheet	-	BLC8G20LS-400AV v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 2 on page 2</a>: changed simplified version drawing SOT1258-3 to SOT1258-1</li> <li>• <a href="#">Table 3 on page 2</a>: changed version SOT1258-3 to SOT1258-1</li> <li>• <a href="#">Figure 13 on page 11</a>: changed package outline drawing SOT1258-3 to SOT1258-1</li> </ul>			
BLC8G20LS-400AV v.3	20161202	Product data sheet	-	BLC8G20LS-400AV v.2
BLC8G20LS-400AV v.2	20150901	Product data sheet	-	BLC8G20LS-400AV v.1
BLC8G20LS-400AV v.1	20150326	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 14. Contact information

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