

# **MELSEC System Q**

Programmable Logic Controllers

User's Manual

## **HART Analog Output Module ME1DA6HAI-Q**





# About this Manual

The texts, illustration, diagrams and examples in this manual are provided for information purposes only. They are intended as aids to help explain the installation, operation, programming and use of the programmable logic controllers of the MELSEC System Q.

If you have any questions about the installation and operation of any of the products described in this manual please contact your local sales office or distributor (see back cover). You can find the latest information and answers to frequently asked questions on our website at [www.mitsubishi-automation.com](http://www.mitsubishi-automation.com).

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# Safety Guidelines

## For use by qualified staff only

This manual is only intended for use by properly trained and qualified electrical technicians who are fully acquainted with the relevant automation technology safety standards. All work with the hardware described, including system design, installation, configuration, maintenance, service and testing of the equipment, may only be performed by trained electrical technicians with approved qualifications who are fully acquainted with all the applicable automation technology safety standards and regulations. Any operations or modifications to the hardware and/or software of our products not specifically described in this manual may only be performed by authorised Mitsubishi Electric staff.

## Proper use of the products

The programmable logic controllers of the MELSEC System Q are only intended for the specific applications explicitly described in this manual. All parameters and settings specified in this manual must be observed. The products described have all been designed, manufactured, tested and documented in strict compliance with the relevant safety standards. Unqualified modification of the hardware or software or failure to observe the warnings on the products and in this manual may result in serious personal injury and/or damage to property. Only peripherals and expansion equipment specifically recommended and approved by Mitsubishi Electric may be used with the programmable logic controllers of the MELSEC System Q.

All and any other uses or application of the products shall be deemed to be improper.

## Relevant safety regulations

All safety and accident prevention regulations relevant to your specific application must be observed in the system design, installation, configuration, maintenance, servicing and testing of these products. The installation should be carried out in accordance to applicable local and national standards. Wiring should follow the HART standards.

## Safety warnings in this manual

In this manual warnings that are relevant for safety are identified as follows:



### **DANGER:**

***Failure to observe the safety warnings identified with this symbol can result in health and injury hazards for the user.***



### **WARNING:**

***Failure to observe the safety warnings identified with this symbol can result in damage to the equipment or other property.***

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## General safety information and precautions

The following safety precautions are intended as a general guideline for using PLC systems together with other equipment. These precautions must always be observed in the design, installation and operation of all control systems.



### **DANGER:**

- **Observe all safety and accident prevention regulations applicable to your specific application. Always disconnect all power supplies before performing installation and wiring work or opening any of the assemblies, components and devices.**
- **Assemblies, components and devices must always be installed in a shockproof housing fitted with a proper cover and fuses or circuit breakers.**
- **Devices with a permanent connection to the mains power supply must be integrated in the building installations with an all-pole disconnection switch and a suitable fuse.**
- **Check power cables and lines connected to the equipment regularly for breaks and insulation damage. If cable damage is found immediately disconnect the equipment and the cables from the power supply and replace the defective cabling.**
- **Before using the equipment for the first time check that the power supply rating matches that of the local mains power.**
- **Take appropriate steps to ensure that cable damage or core breaks in the signal lines cannot cause undefined states in the equipment.**
- **You are responsible for taking the necessary precautions to ensure that programs interrupted by brownouts and power failures can be restarted properly and safely. In particular, you must ensure that dangerous conditions cannot occur under any circumstances, even for brief periods.**
- **EMERGENCY OFF facilities conforming to EN 60204/IEC 204 and VDE 0113 must remain fully operative at all times and in all PLC operating modes. The EMERGENCY OFF facility reset function must be designed so that it cannot ever cause an uncontrolled or undefined restart.**
- **You must implement both hardware and software safety precautions to prevent the possibility of undefined control system states caused by signal line cable or core breaks.**
- **When using modules always ensure that all electrical and mechanical specifications and requirements are observed exactly.**
- **At power ON/OFF, current may instantaneously be output from the output terminal of this module. In such case, wait until the analog output becomes stable to start controlling the external device.**



# Contents

<b>1</b>	<b>Overview</b>	
1.1	Features .....	1-1
<b>2</b>	<b>System Configuration</b>	
2.1	Applicable Systems.....	2-1
2.2	How to Check the Function Version and Serial No. of the Modules .....	2-3
<b>3</b>	<b>Detailed Description of the Module</b>	
3.1	Part Names.....	3-1
3.1.1	Signal Layout of the Terminal Block .....	3-2
3.2	Specifications .....	3-3
3.2.1	I/O conversion characteristics .....	3-4
3.2.2	Accuracy .....	3-5
3.2.3	External Dimensions .....	3-5
3.3	Functions of the HART Analog Output Module .....	3-6
3.3.1	Analog output HOLD/CLEAR function .....	3-6
3.3.2	Analog output test during PLC CPU STOP.....	3-8
3.3.3	Rate control function .....	3-8
3.3.4	Scaling function .....	3-10
3.3.5	Warning output function .....	3-11
3.3.6	Disconnection detection function.....	3-12
3.3.7	Short circuit detection function .....	3-13
3.3.8	HART Master Function .....	3-14
3.4	I/O Signals for the Programmable Controller CPU.....	3-16
3.4.1	List of I/O signals .....	3-16
3.4.2	Details of I/O signals .....	3-17
3.5	Buffer Memory .....	3-20
3.5.1	Buffer memory assignment .....	3-21
3.5.2	CH□ digital value (Un\G1 to Un\G6) .....	3-32
3.5.3	CH□ set value check codes (Un\G11 to Un\G16).....	3-33
3.5.4	Error code (Un\G19) .....	3-33
3.5.5	Setting range (Un\G20, Un\G21).....	3-33

3.5.6	Short circuit detection setting (Un\G45) .....	3-34
3.5.7	Rate control enable/disable setting (Un\G46) .....	3-34
3.5.8	Disconnection detection/warning output setting (Un\G47) .....	3-35
3.5.9	Warning output flags (Un\G48).....	3-35
3.5.10	Disconnection detection flags (Un\G49) .....	3-36
3.5.11	Short circuit detection flag (Un\G50) .....	3-36
3.5.12	Scaling enable/disable setting (Un\G53).....	3-37
3.5.13	CHI scaling upper/lower limit values (Un\G54 to Un\G65) .....	3-37
3.5.14	CHI Increase/decrease digital limit values (Un\G70 to Un\G81) .....	3-37
3.5.15	CHI Warning output upper/lower limit values (Un\G86 to Un\G97) .....	3-38
3.5.16	HART enable (Un\G160).....	3-38
3.5.17	HART scan list (Un\G161).....	3-38
3.5.18	HART cycle time (Un\G162 to Un\G164) .....	3-39
3.5.19	HART maximum retries (Un\G176 to Un\G181).....	3-40
3.5.20	HART device information refresh interval (Un\G191) .....	3-40
3.5.21	HART field device status (Un\G240, Un\G252, Un\G264...) .....	3-40
3.5.22	Extended HART field device status (Un\G241, Un\G253, Un\G265...) .....	3-41
3.5.23	Device variable status (Un\G242 & Un\G243, Un\G254 & Un\G255...) .....	3-42
3.5.24	HART process variables (Un\G244 to Un\G251, Un\G256 to Un\G263...) .....	3-43
3.5.25	HART Command Request (Un\G352 to Un\G483) .....	3-44
3.5.26	HART Command Answer (Un\G496 to Un\G627) .....	3-46
3.5.27	Information about HART Device (Un\G896 to Un\G966, Un\G968 to Un\G1038...).....	3-47

## **4 Setup and Procedures before Operation**

4.1	Handling Precautions.....	4-1
4.2	Setup and Procedures before Operation .....	4-2
4.3	Installation of the Module .....	4-3
4.4	Wiring .....	4-4
4.4.1	Wiring precautions .....	4-4
4.4.2	External wiring .....	4-5
4.5	PLC Parameter Setting.....	4-6
4.5.1	I/O assignment .....	4-6
4.5.2	Intelligent function module switch settings.....	4-7
4.6	Setting of the HART Devices .....	4-9

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<b>5</b>	<b>Intelligent Function Utility (GX Works2)</b>	
5.1	Addition of a new Module to the Project.....	5-1
5.2	Switch Setting .....	5-3
5.3	Parameter Setting .....	5-5
5.4	Auto Refresh Settings .....	5-7
5.5	Writing the Intelligent Function Module Settings to the PLC.....	5-8
<b>6</b>	<b>Programming</b>	
6.1	Programming Procedure.....	6-1
6.2	Example 1: ME1DA6HAI-Q combined with PLC CPU .....	6-3
6.2.1	Before creating a program.....	6-4
6.2.2	Program .....	6-7
6.3	Example 2: ME1DA6HAI-Q used in Remote I/O Network.....	6-13
6.3.1	Before creating a program.....	6-14
6.3.2	Network parameter .....	6-17
6.3.3	Program .....	6-20
<b>7</b>	<b>Troubleshooting</b>	
7.1	Error Code List .....	7-1
7.2	Troubleshooting using the LEDs of the Module .....	7-2
7.2.1	When the "RUN" LED is flashing or turned off.....	7-2
7.2.2	When the "ERR." LED is on .....	7-2
7.2.3	When the "ALM" LED is on or flashing.....	7-2
7.3	When an Analog Output Value is Not Output .....	7-3
7.4	When an Analog Output Value is Not Held.....	7-3
7.5	Checking the Analog Output Module Status .....	7-4
	<b>Index</b>	



# 1 Overview

This User's Manual describes the specifications, handling and programming methods for the HART analog output module ME1DA6HAI-Q (hereinafter referred to as the ME1DA6HAI-Q) which is used with the CPU modules of the MELSEC System Q. The ME1DA6HAI-Q is exclusively used for current output.

## 1.1 Features

### **Multi-channel analog output is available.**

By using a single ME1DA6HAI-Q, analog current outputs of 6 points (6 channels) are available. Standard devices with 4 to 20 mA or 0 to 20 mA input range and HART devices can be connected to the module at the same time. The analog output range of the ME1DA6HAI-Q is selectable by the intelligent function module switch setting in GX(IEC) Developer.

### **HART master function**

The ME1DA6HAI-Q can communicate with up to six HART-enabled devices. (One HART device connected to each channel.) HART\* is a bi-directional industrial field communication protocol used to communicate between intelligent field devices and host systems.

For this communication no additional wiring is required. Additional device information is communicated using a digital signal that is superimposed on the analog signal. The digital signal contains information from and to the device including device configuration or re-configuration, device status, diagnostics, or additional information.

The ME1DA6HAI-Q can operate as a HART master with protocol revision 6.

\* HART stands for **H**ighway **A**ddressable **R**emote **T**ransducer. For more information about the HART protocol please refer to section 3.3.6.

### **FDT/DTM function support**

The FDT/DTM\* can be used for setting and monitoring the HART devices. To use this function, the HART device must have DeviceDTM.

\* FDT stands for **F**ield **D**evice **T**ool and DTM stands for **D**evice **T**ype **M**anager. FDT/DTM is a communication technique for the manufacturer-independent configuration of processing systems at a field bus.

### **High accuracy**

The accuracy is as high as  $\pm 0.3\%$  over the specified operating temperature range for the MELSEC System Q.

### **Easy changing of the output range**

The output range (4 to 20 mA or 0 to 20 mA) can easily be set from the GX (IEC) Developer.

### **Analog output hold/clear function**

This function is used to set whether the analog output value will be held or cleared when the PLC CPU module is in a STOP status or when an error occurs which stops the PLC CPU.

### **Warning output function**

A warning is triggered if a digital input value falls outside the setting range.

### **Rate control function**

The increment and decrement of the analog output value per conversion cycle can be restricted.

**Disconnection detection function**

When the analog output current is 4mA or more, the voltage across the output is watched to detect a disconnection.

**Short circuit detection function**

When the analog output current is 4 mA or more, the external load resistance is watched to detect a short circuit.

**Scaling function**

The digital input value range (Un\G1–Un\G6) can be changed to any given range between –32768 and 32767, and digital values within the range are converted to analog values.

**Easy settings using the "Intelligent function utility"**

The "Intelligent function utility" is not a required item, however, it is useful for on-screen setting of the intelligent function module parameters (initial setting/auto refresh setting).\*

\* The "Intelligent function utility" is supported by the ME1DA6HAI-Q if the first 5 digits of the serial number are "14102" or higher.

# 2 System Configuration

## 2.1 Applicable Systems

### Applicable modules, base units, and No. of modules

- When mounted with a CPU module

The table below shows the CPU modules and base units applicable to the HART Analog Output Module ME1DA6HAI-Q and quantities for each CPU model.

Depending on the combination with other modules or the number of mounted modules, the power supply capacity may be insufficient. Pay attention to the power supply capacity before mounting modules, and if the power supply capacity is insufficient, change the combination of the modules.

Applicable CPU module		No. of ME1DA6HAI-Q that can be installed*1	Base unit*2		
CPU type	CPU model		Main base unit	Extension base unit	
Programmable controller CPU	Basic model QCPU	Q00JCPU	Up to 16	●	●
		Q00CPU	Up to 24	●	●
		Q01CPU			
	High performance model QCPU	Q02CPU	Up to 64	●	●
		Q02HCPU			
		Q06HCPU			
		Q12HCPU			
	Process CPU	Q02PHCPU	Up to 64	●	●
		Q06PHCPU			
		Q12PHCPU			
		Q25PHCPU			
	Redundant CPU	Q12PRHCPU	Up to 53	○	●
		Q25PRHCPU			
	Universal model QCPU	Q00UJCPU	Up to 16	●	●
		Q00UCPU	Up to 24		
		Q01UCPU	Up to 36		
		Q02UCPU	Up to 64		
		Q□UD(E)CPU			
		Q50UDEHCPU			
Q100UDEHCP					
Safety CPU	QS001CPU	—	○	○	
C Controller module	Q06CCPU-V-H01	Up to 64	●	●	
	Q06CCPU-V				
	Q06CCPU-V-B				
	Q12DCCPU-V				

**Tab. 2-1:** Applicable base units and number of mountable modules

● : Applicable, ○: N/A

\*1 Limited within the range of I/O points for the CPU module.

\*2 The ME1DA6HAI-Q can be installed to any I/O slot of a base unit.

**NOTE**

A ME1DA6HAI-Q can not installed at the main base in a redundant system with QnPRHCPU.

- Mounting to a MELSECNET/H remote I/O station

The table below shows the network modules and base units applicable to the analog output module ME1DA6HAI-Q and quantities for each network module model.

Depending on the combination with other modules or the number of mounted modules, power supply capacity may be insufficient. Pay attention to the power supply capacity before mounting modules, and if the power supply capacity is insufficient, change the combination of the modules.

Applicable network module	No. of ME1DA6HAI-Q that can be installed*1	Base unit*2	
		Main base unit of remote I/O station	Extension base unit of remote I/O station
QJ72LP25-25	Up to 64	●	●
QJ72LP25G			
QJ72LP25GE			
QJ72BR15			

**Tab. 2-2:** Applicable base units and number of mountable modules in a MELSECNET/H remote I/O station

● : Applicable, ○ : N/A

\*1 Limited within the range of I/O points for the network module.

\*2 The ME1DA6HAI-Q can be installed to any I/O slot of a base unit.

**NOTE**

The Basic model QCPU or C Controller module cannot create the MELSECNET/H remote I/O network.

### Support of the multiple CPU system

The function version of the HART analog output module supports the multiple CPU system. When using the ME1DA6HAI-Q in a multiple CPU system, refer to the following manual first.

- QCPU User's Manual (Multiple CPU System)

- Intelligent function module parameters

Write intelligent function module parameters to only the control CPU of the ME1DA6HAI-Q.

### Compatibility with online module change

The ME1DA6HAI-Q does not support online module change.

### Supported software packages

For setting the PLC parameters for a system containing the ME1DA6HAI-Q and programming, the software packages GX Developer, GX IEC Developer and GX Works2 can be used.

In addition, the Intelligent Function Utility of GX Works2 can be used to set the intelligent function module parameters (initial settings/auto refresh settings) of the ME1DA6HAI-Q.

Depending on the CPU module used, a certain version of the software is needed since newly CPU modules are not supported by previous versions.

**NOTE**

Please check whether the mounted CPU module is supported or not by your version of the programming software.



## 2.2 How to Check the Function Version and Serial No. of the Modules

Using the programming software GX Developer, GX IEC Developer or GX Works2, the serial No. and the function version can be checked while the PLC is operating.

From the **Diagnostics** menu select **System Monitor** and then select **Product Inf. List**.

Slot	Type	Series	Model name	Points	I/O No.	Master PLC	Serial No	Ver.
PLC	PLC	Q	Q02HCPU	-	-	-	0212200000000000	B
0-0	Intelli. Q	Q	026ME1DA6HAI-Q	32pt	0000	-	1203100000000000	B

**Fig. 2-1:** Product Information List for a PLC with a ME1DA6HAI-Q

**NOTE**

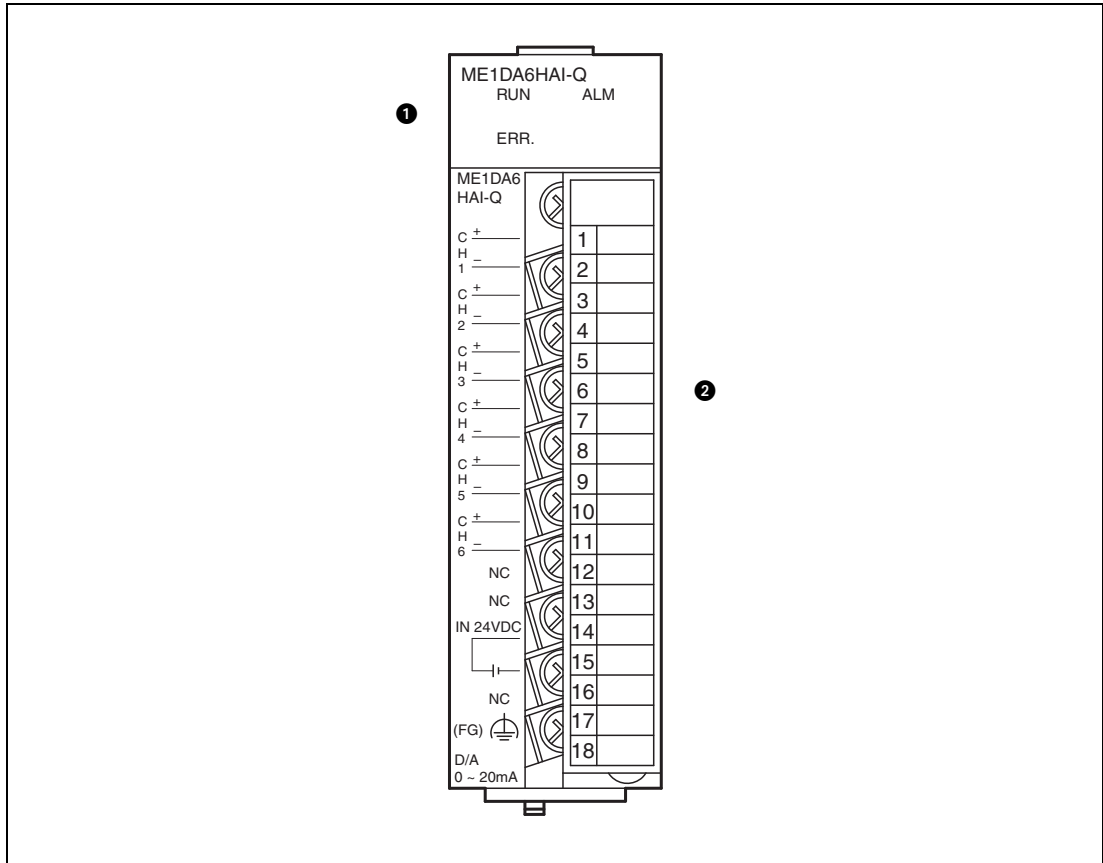
The serial number displayed on the product information screen of GX Developer, GX IEC Developer or GX Works2 describes the function information of the product. The function information of the product is updated when a new function is added.



# 3 Detailed Description of the Module

## 3.1 Part Names

This section explains the names of the components for the ME1DA6HAI-Q.



**Fig. 3-1:** Names of parts

No.	Name	Description
①	LEDs	RUN On: Normal operation Flashing: Intelligent function module setting switch 4 is not set to "0". Off: - Power supply (5 V DC) is off - A watchdog timer error has occurred.
		ERR. On: Operation error Off: Normal operation
		ALM On: A short circuit at an analog output has been detected. Flashing: A disconnection at an analog output has been detected. Off: Normal operation
②	Detachable terminal block	Used for connection of the HART current input devices (slaves) or normal current input devices and the external power supply.

**Tab. 3-1:** Description of the LEDs and the terminal block of the ME1DA6HAI-Q

**NOTE**

When two or more errors have occurred, the latest error found by the HART analog output module is indicated with the LED.

### 3.1.1 Signal Layout of the Terminal Block

Terminal No.	Signal name	Description
1	CH1	+
2		-
3	CH2	+
4		-
5	CH3	+
6		-
7	CH4	+
8		-
9	CH5	+
10		-
11	CH6	+
12		-
13	NC	Not connected
14	NC	
15	+ 24 V DC	External power supply
16	0 V	
17	NC	Not connected
18	(FG)	Frame Ground

**Tab. 3-2:** Signal layout for the detachable terminal block of the ME1DA6HAI-Q

For the wiring of the HART analog output module ME1DA6HAI-Q please refer to section 4.4.

## 3.2 Specifications

The specifications for the ME1DA6HAI-Q are shown in the following table. For general specifications, refer to the operation manual for the CPU module being used.

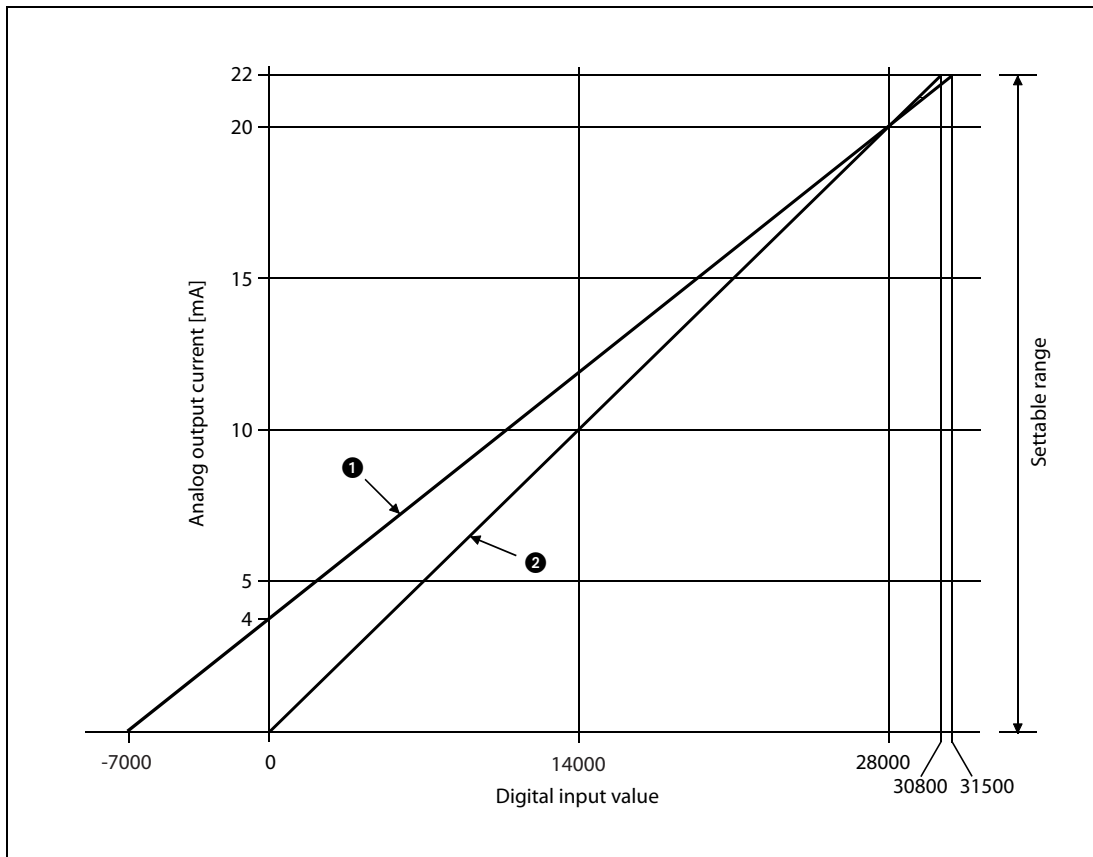
Item		Specifications								
Number of analog outputs		6 points (6 channels)								
Analog output	Current	0 to 20 mA DC								
	External load	50 to 600 Ω								
Digital input		16-bit signed binary (–32768 to 32767)								
I/O characteristics, maximum resolution		<table border="1"> <thead> <tr> <th>Analog output range</th> <th>Digital input value</th> <th>Maximum resolution</th> </tr> </thead> <tbody> <tr> <td>0 to 20 mA</td> <td rowspan="2">0 to 28000</td> <td>714 nA</td> </tr> <tr> <td>4 to 20 mA</td> <td>571 nA</td> </tr> </tbody> </table>	Analog output range	Digital input value	Maximum resolution	0 to 20 mA	0 to 28000	714 nA	4 to 20 mA	571 nA
		Analog output range	Digital input value	Maximum resolution						
		0 to 20 mA	0 to 28000	714 nA						
4 to 20 mA	571 nA									
Accuracy (relative to the analog output range)	Ambient temperature 25 °C ±5 °C	±0.15% (±42 digit)								
	Ambient temperature 0 to 55 °C	±0.3 % (±84 digit)								
Conversion time	with HART	220 ms <sup>①</sup> (Independent to the number of used channels)								
	without HART	70 ms (Independent to the number of used channels)								
Protection functions <sup>②</sup>	Disconnection detection	When the output voltage is higher than 15 V.								
	Short circuit detection	When the external load is <30 Ω.								
	Response time	0.5 seconds for all channels (Independent to the number of used channels)								
Insulation method	Between the I/O terminals and PLC power supply	Digital isolator insulation								
	Between analog output channels	Non-insulated								
	Between I/O terminals and external power supply	Transformer insulation								
HART modem		FSK Physical Layer, multiplexed								
HART functions		– Protocol Revision 6 support – 4 Process variables support (PV, SV, TV, QV) – FDT/DTM support								
Number of I/O occupied points		32 points (I/O assignment: Intelligent 32 points)								
External wiring connection system		18-points terminal block								
Applicable wire size		Refer to the HART specification for more details. <sup>③</sup>								
Applicable solderless terminals		R1.25-3 (Solderless terminals with sleeves cannot be used.)								
External supply power	Voltage	24 V DC (+20%, -15%); ripple, spike within 500mV <sub>P-P</sub>								
	Current	0.28 A								
	Inrush current	5.3 A within 100 μs								
Online module change		Not supported								
Internal current consumption (5 VDC)		0.32 A								
Weight		0.19 kg								

**Tab. 3-3:** Specifications of the ME1DA6HAI-Q

- <sup>①</sup> In the PLC parameters (intelligent function module switches) the conversion time with HART communication can be set to the same value as the conversion time without HART communication (refer to section 4.5.2).
- <sup>②</sup> The protection functions can only be used with output currents of 4 mA or more.
- <sup>③</sup> Use case:  
For distances up to 800 m, the wire size of 0.51 mm diameter with 115 nF/km cable capacitance and 36.7 Ω/km cable resistance can be applied.

### 3.2.1 I/O conversion characteristics

The I/O conversion characteristics are used for converting the digital value written from the PLC CPU to an analog output value (current output). In the following figure the I/O conversion characteristics are represented by inclined straight lines.



**Fig. 3-2:** Current output characteristics of the ME1DA6HAI-Q

No.	Output range setting	Digital input value		Resolution
		Normal range	Tight shut off	
1	4 to 20 mA	-7000 to 28000	31500	571 nA
2	0 to 20 mA	0 to 28000	30800	714 nA

**Tab. 3-4:** Shut-off values and resolution for the various output ranges

**NOTES**

Digital input values below 0 in the 4 to 20 mA setting range will result in output currents smaller than 4 mA.

Negative output currents are not allowed.

Choose the appropriate analog output range for each channel according to the specifications of the connected device.

If these ranges are exceeded, the maximum resolution and accuracy may not fall within the performance specifications.

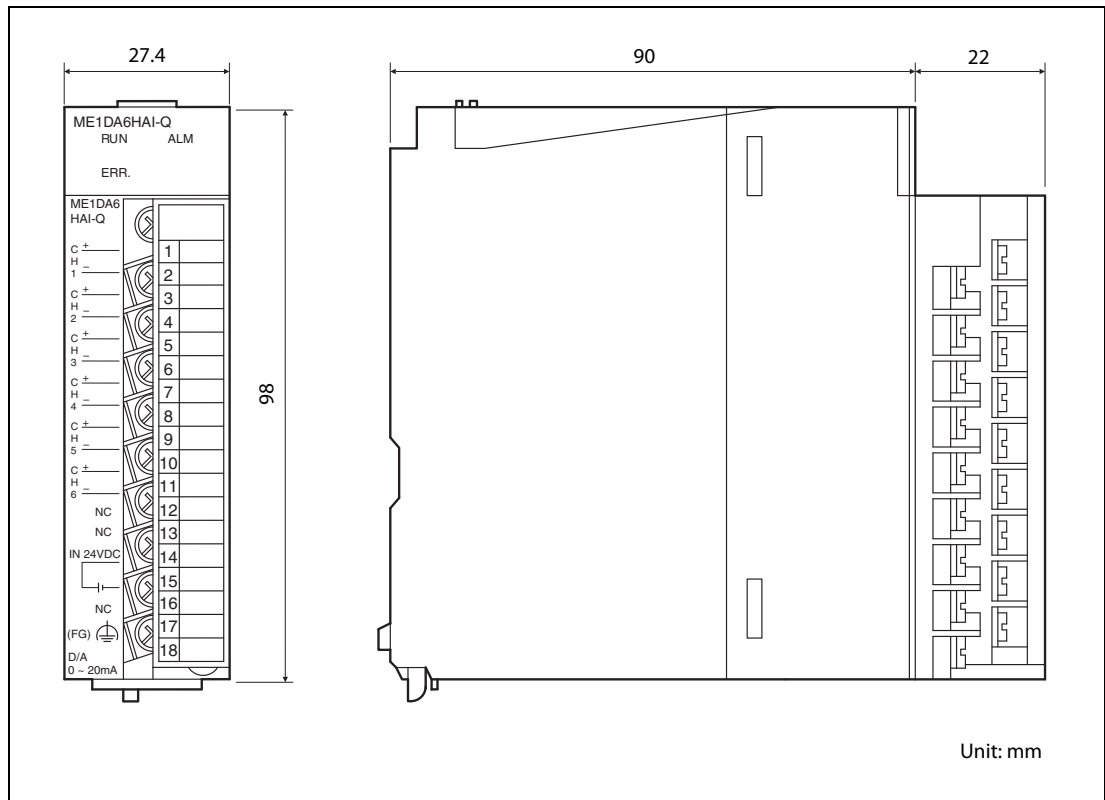
### 3.2.2 Accuracy

The reference accuracy is the accuracy relative to the analog output range.

Even if the analog output range is changed to change the output characteristic, the reference accuracy does not vary and is kept within the range given in the performance specifications.

An accuracy of  $\pm 0.3\%$  is maintained over the whole operating temperature range of the MELSEC System Q (0 to +55 °C).

### 3.2.3 External Dimensions



**Fig. 3-3:** Dimensions of the ME1DA6HAI-Q

### 3.3 Functions of the HART Analog Output Module

Function	Description	Reference
Analog output HOLD/CLEAR	The output analog value can be retained when the PLC CPU module is placed in the STOP status or when an error occurs.	Section 3.3.1
Analog output test during PLC CPU STOP	When the CH□ output enable/disable flag is forced ON during PLC CPU STOP, the D/A converted analog value is output	Section 3.3.2
Rate control	The increment and decrement of the analog output value per conversion cycle can be restricted.	Section 3.3.3
Scaling	The input range of digital values can be changed to any given range between -32768 and 32767.	Section 3.3.4
Warning output	A warning is triggered if a digital input value falls outside the setting range.	Section 3.3.5
Disconnection detection	When the analog output current is 4 mA or more, the voltage across the output is watched to detect a disconnection.	Section 3.3.6
Short-circuit detection	When the analog output current is 4 mA or more, the external load resistance is monitored to detect a short circuit on a channel.	Section 3.3.7
HART Master function	<ul style="list-style-type: none"> <li>HART communication support The ME1DA6HAI-Q can communicate with up to six HART-enabled devices. (One HART device connected to each channel.) Communication occurs using standard instrumentation grade wire and using standard wiring and termination practices – no additional wiring is required.</li> <li>FDT/DTM function support Using a commercially available FDT (Field Device Tool), reading/writing the HART device's parameters and monitoring the HART device status are executable via the ME1DA6HAI-Q.</li> </ul>	Section 3.3.8

**Tab. 3-5:** Functions of the ME1DA6HAI-Q

#### 3.3.1 Analog output HOLD/CLEAR function

For the case where the programmable controller (PLC) CPU is placed in STOP or in a stop error status, whether to hold (HOLD) or clear (CLEAR) the analog output value can be set.

Make the setting in the HOLD/CLEAR setting of the intelligent function module switch (please refer to section 4.5.2).

Depending on combinations of the HOLD/CLEAR setting, the CH□ output enable/disable flag (Y1 to Y6), the analog output range setting and whether HART communication is enabled or not, the analog output status varies as shown in the following tables.

#### NOTE

The offset value for the 4 to 20 mA range is 4 mA. Output currents lesser than 4 mA will be overwritten with a higher value (4 mA) in case of e.g. "PLC CPU stop error" (refer to the following table). Therefore for output currents lesser than 4 mA it is recommended to use the 0 to 20 mA range.



Setting combination / Execution status	Analog output for HART communication <sup>*3</sup>	Enable <sup>*3</sup>			Disable		
	CH $\square$ output enable/disable flags (Y1 to Y6)	Enable		Disable	Enable		Disable
	HOLD/CLEAR setting	HOLD	CLEAR	HOLD or CLEAR	HOLD	CLEAR	HOLD or CLEAR
PLC CPU is in RUN	HART communication	Possible <sup>*3</sup>			Not possible		
	Analog output	Analog value of the D/A converted digital value <sup>*2</sup>		Offset value (4 mA)	Analog value of the D/A converted digital value <sup>*2</sup>		0 mA
PLC CPU is in STOP	HART communication	Possible <sup>*3</sup>			Not possible		
	Analog output	Last value	Offset value (4 mA)		Last value	Offset value (4 mA)	0 mA
PLC CPU stop error occurred	HART communication	Possible <sup>*3</sup>			Not possible		
	Analog output	Last value	Offset value (4 mA)		Last value	Offset value (4 mA)	0 mA
Watchdog timer error <sup>*1</sup> occurred	HART communication	Not possible			Not possible		
	Analog output	0 mA			0 mA		

**Tab. 3-6:** HART communication and analog output in dependence of the setting combinations (output range: 4 to 20 mA)

- \*1 A watchdog timer error occurs when program operations are not completed within the scheduled time due to a hardware problem of the D/A module. In this case, the module ready signal (X0) and the D/A module RUN LED are turned off.
- \*2 The rate control and scaling function is activated.
- \*3 HART communication will be stopped without notification for output currents lesser than 2 mA. It will recover automatically if the output current is 2 mA or higher again (refer to section 3.5.16).

Setting combination / Execution status	Analog output for HART communication <sup>*3</sup>	Enable <sup>*3</sup>			Disable		
	CH $\square$ output enable/disable flags (Y1 to Y6)	Enable		Disable	Enable		Disable
	HOLD/CLEAR setting	HOLD	CLEAR	HOLD or CLEAR	HOLD	CLEAR	HOLD or CLEAR
PLC CPU is in RUN	HART communication	Possible <sup>*3</sup>			Not possible		
	Analog output	Analog value of the D/A converted digital value <sup>*2</sup>		0 mA	Analog value of the D/A converted digital value <sup>*2</sup>		0 mA
PLC CPU is in STOP	HART communication	Possible <sup>*3</sup>			Not possible		
	Analog output	Last value	0 mA		Last value	0 mA	
PLC CPU stop error occurred	HART communication	Possible <sup>*3</sup>			Not possible		
	Analog output	Last value	0 mA		Last value	0 mA	
Watchdog timer error <sup>*1</sup> occurred	HART communication	Not possible			Not possible		
	Analog output	0 mA			0 mA		

**Tab. 3-7:** HART communication and analog output in dependence of the setting combinations (output range: 0 to 20 mA)

- \*1 A watchdog timer error occurs when program operations are not completed within the scheduled time due to a hardware problem of the D/A module. In this case, the module ready signal (X0) and the D/A module RUN LED are turned off.
- \*2 The rate control and scaling function is activated.
- \*3 HART communication will be stopped without notification for output currents lesser than 2 mA. It will recover automatically if the output current is 2 mA or higher again (refer to section 3.5.16).

**NOTE**

The following conditions should be satisfied when the analog output HOLD/CLEAR function is used on a MELSECNET/H remote I/O station.

- The master module of function version D or later and the remote I/O module of function version D or later are required.
- Validate the station unit block guarantee of the send side cyclic data. (Refer to the Q Corresponding MELSECNET/H Network System Reference Manual).
- The setting for holding the output in the case of a link error must be made in the column "Error time output mode" in the I/O assignment setting (Refer to section 4.5.1). The HOLD/CLEAR setting by the intelligent function module switch is invalid.

This setting is validated on a per-module basis, and is not made on a per channel basis. Therefore, to make the output status at a stop error or STOP of the programmable controller CPU matched with the output status at a link error, set the same HOLD/CLEAR setting to all channels (Refer to the table below.)

Output status	Setting of "Error time output mode"	HOLD/CLEAR setting (Same setting to all channels)
Hold analog output	HOLD	HOLD
Clear analog output (Output offset value)	CLEAR	CLEAR

### 3.3.2 Analog output test during PLC CPU STOP

During the programmable controller CPU STOP, an analog value can be output to test the correct function of the D/A module. The test is enabled by the CH□ output enable/disable flag (Y1 to Y6) as shown in the following table.

	CH□ output enable/disable flag (Y1 to Y6)	
	Enable	Disable
Analog output test	Allowed	Not allowed

**Tab. 3-8:** An analog output test is enabled by the output enable/disable flag

To conduct an analog output test, perform the following operations in GX Developer device testing:

- Set the output enable/disable flag (Y1 to Y6) for the channel to be tested to "Enable" (OFF → ON).
- Write a digital value equivalent to the analog value to be output in CH□ digital value in the buffer memory (buffer memory addresses Un\G1 to Un\G6, refer to section 3.5.2).

### 3.3.3 Rate control function

The increment and decrement of the analog output value per conversion cycle (10 ms) are restricted to prevent a sudden change of the analog output value.

The rate control can be enabled or disabled for each channel by the rate control enable/disable setting (buffer memory address Un\G46). To enable rate control, write "0" to the bit position corresponding to the channel number and turn ON the operating condition setting request (Y9). As default, rate control is disabled for all channels.

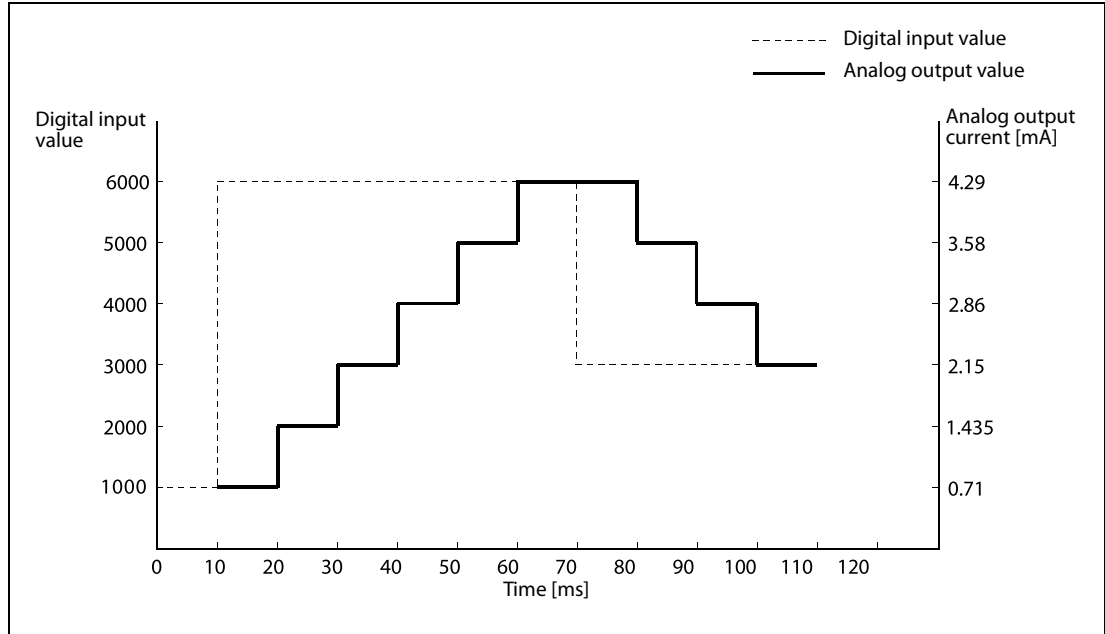
The increase digital limit value and decrease digital limit value are set in the buffer memory addresses Un\G70 to Un\G81.

If HART communication is enabled the rate control function is applied to before the output signal is filtered by the FIR filter.

Example:

- Output range: 0 to 20 mA
- Increase digital limit value: 1000
- Decrease digital limit value: 1000

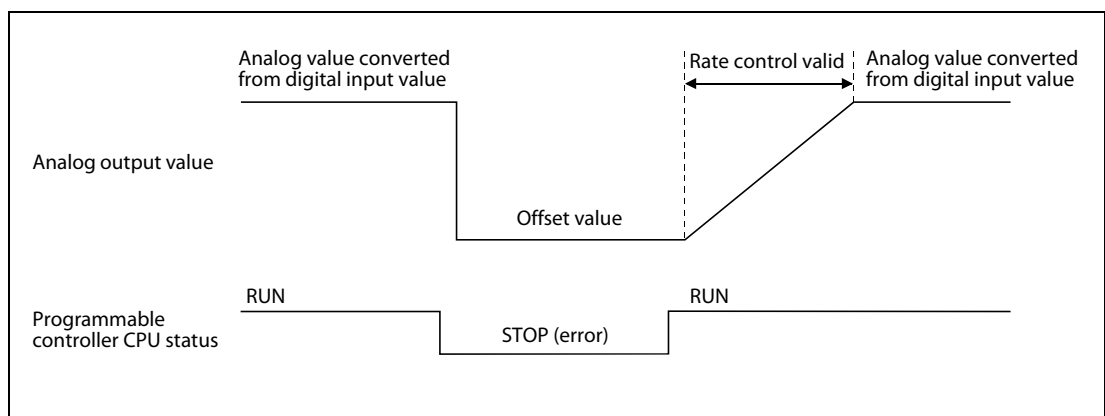
The control example in this case is indicated below.



**Fig. 3-4:** Example for the rate control function

If the operation of the programmable controller CPU varies at the setting of D/A output enable and analog output clear, the rate control functions as indicated below.

- If the programmable controller CPU has switched from RUN to STOP (error): Rate control does not function.
- If the programmable controller CPU has switched from STOP (error) to RUN: Rate control functions.



**Fig. 3-5:** Rate control function when the PLC CPU has switched to STOP or RUN.

### 3.3.4 Scaling function

The scaling function can be enabled individually for each channel by setting the corresponding bit in buffer memory address Un\G53.

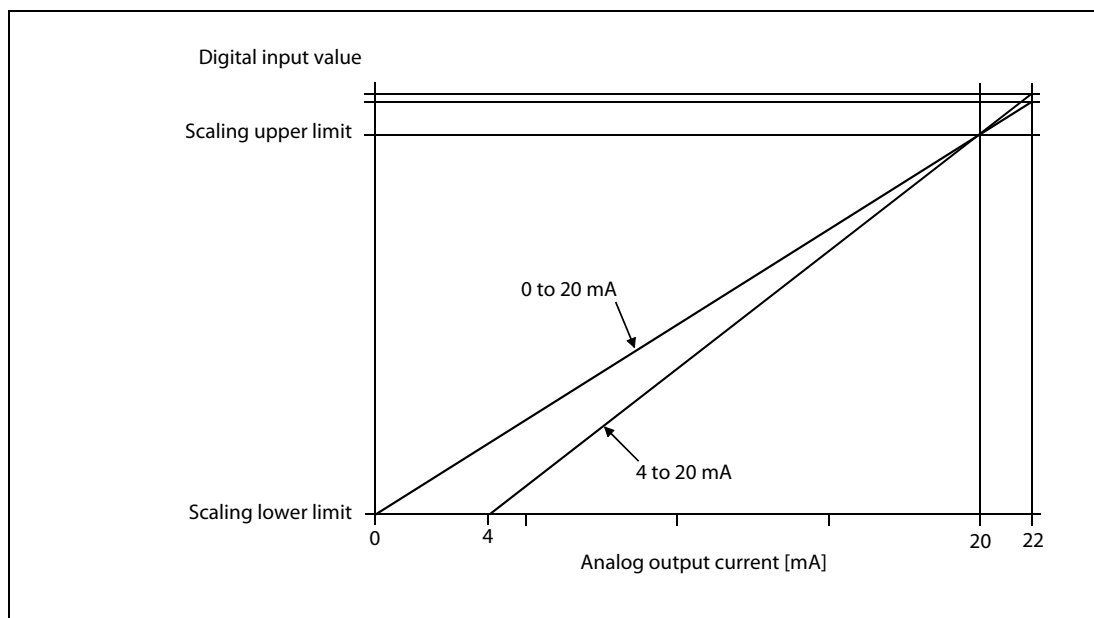
With this function, the input range of a digital value can be changed into arbitrary ranges between -32768 and 32767.

A digital input value stored in CH□ scaling value (buffer memory addresses Un\G1 to Un\G6) is converted from the range set by CH□ scaling upper/lower limit value (buffer memory addresses Un\G54 to Un\G65) into the analog output range.

Digital input values which equal analog outputs up to 22 mA are allowed (The limit for the digital input value is 32767). Outputs greater than 22 mA will result in an error.

For both ranges, digital input values which equal analog outputs down to 0 mA are allowed (The limit for the digital input value is -32768). Outputs smaller than 0 mA will result in an error.

When the warning function is used (refer to section 3.3.5), input values converted within the scaling range are checked for warning output.



**Fig. 3-6:** Scaling function of the ME1DA6HAI-Q

### 3.3.5 Warning output function

If the digital input value written to the buffer memory (addresses Un\G1 to Un\G6) is equal to or greater than the warning output upper limit value or is equal to or less than the warning output lower limit value, the warning output flag (buffer memory address Un\G48) and warning output signal (XE) turn ON to give a warning. The warning is triggered for the D/A conversion enabled channel only. For a description of the warning output upper/lower limit value, please refer to section 3.5.15.

The warning output flag will be set if one of the following conditions is fulfilled:

- *Warning output lower limit  $\geq$  digital value*
- *Warning output upper limit  $\leq$  digital value*

At occurrence of the warning, the analog output value is converted from the digital value at the warning output upper limit value or warning output lower limit value.

The warning output flag (buffer memory address Un\G48) and warning output signal (XE) turn OFF when the operating condition setting request (Y9) or warning output clear request (YE) turns ON.

For each channel, the warning output can be enabled or disabled by the disconnection detection/warning output setting (buffer memory address Un\G47). To enable the warning output, write "0" to the bit position corresponding to the channel number and turn ON the operating condition setting request (Y9). As default warning output is disabled for all channels.

Set the warning output upper and lower limit values to the buffer memory addresses Un\G86 to Un\G97. When the scaling function is used, input values converted within the scaling range are checked for warning output.

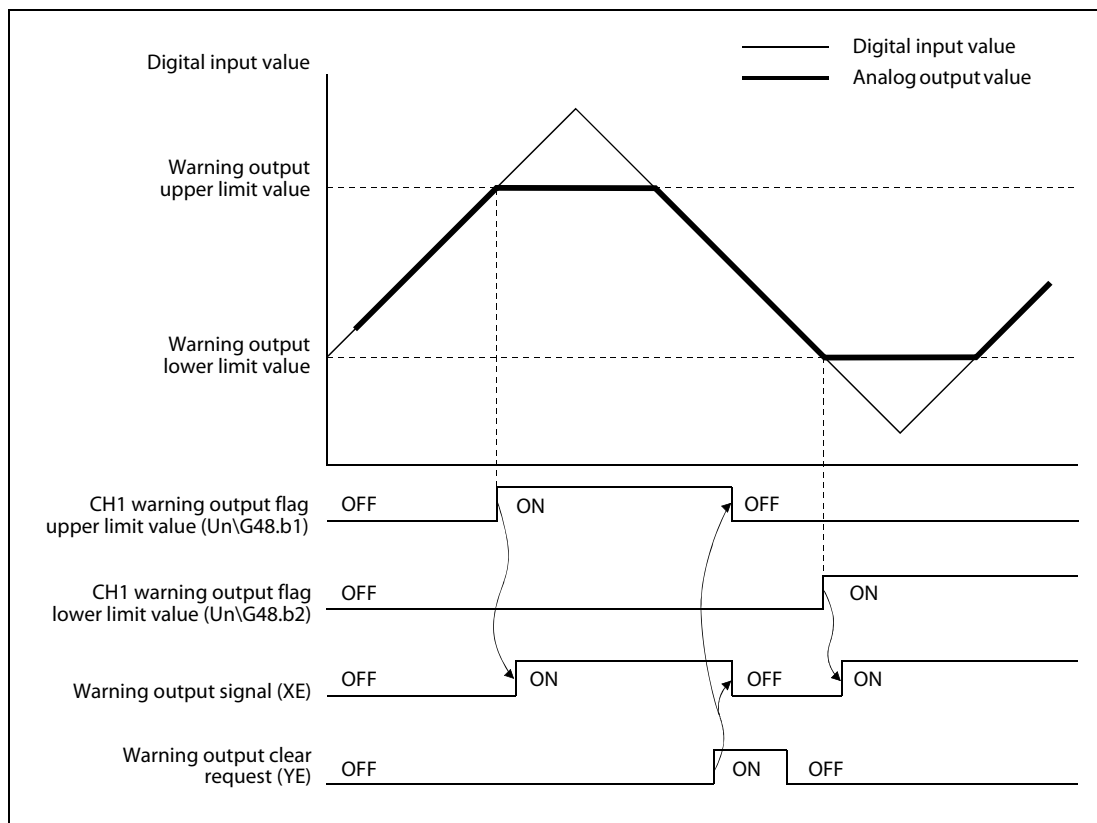


Fig. 3-7: Example for the warning output function

**NOTES**

If the warning is triggered immediately after D/A conversion is enabled, make a warning output clear request after writing the digital value that is less than the warning output upper limit value and is greater than the warning output lower limit value.

During an analog output test, the warning output function is invalid.

### 3.3.6 Disconnection detection function

When the output voltage increases to 15 V or more while an output current of 4 mA or more is set, a disconnection is detected and both the disconnection detection flag (buffer memory address Un\G49) and disconnection detection signal (XD) turn ON. The disconnection is also signaled by the flashing ALM LED. Disconnection is detected only on a channel set for D/A output enable.

The disconnection detection flag (buffer memory address Un\G49) and disconnection detection signal (XD) turn OFF when the operating condition setting request (Y9) or disconnection detection clear request (YD) turns ON.

The disconnection detection function can be enabled or disabled for each channel by the disconnection detection/warning output setting (buffer memory address Un\G47). To enable the disconnection detection, write "0" to the bit position corresponding to the channel number and turn ON the operating condition setting request (Y9). Disconnection detection is disabled for all channels as a default.

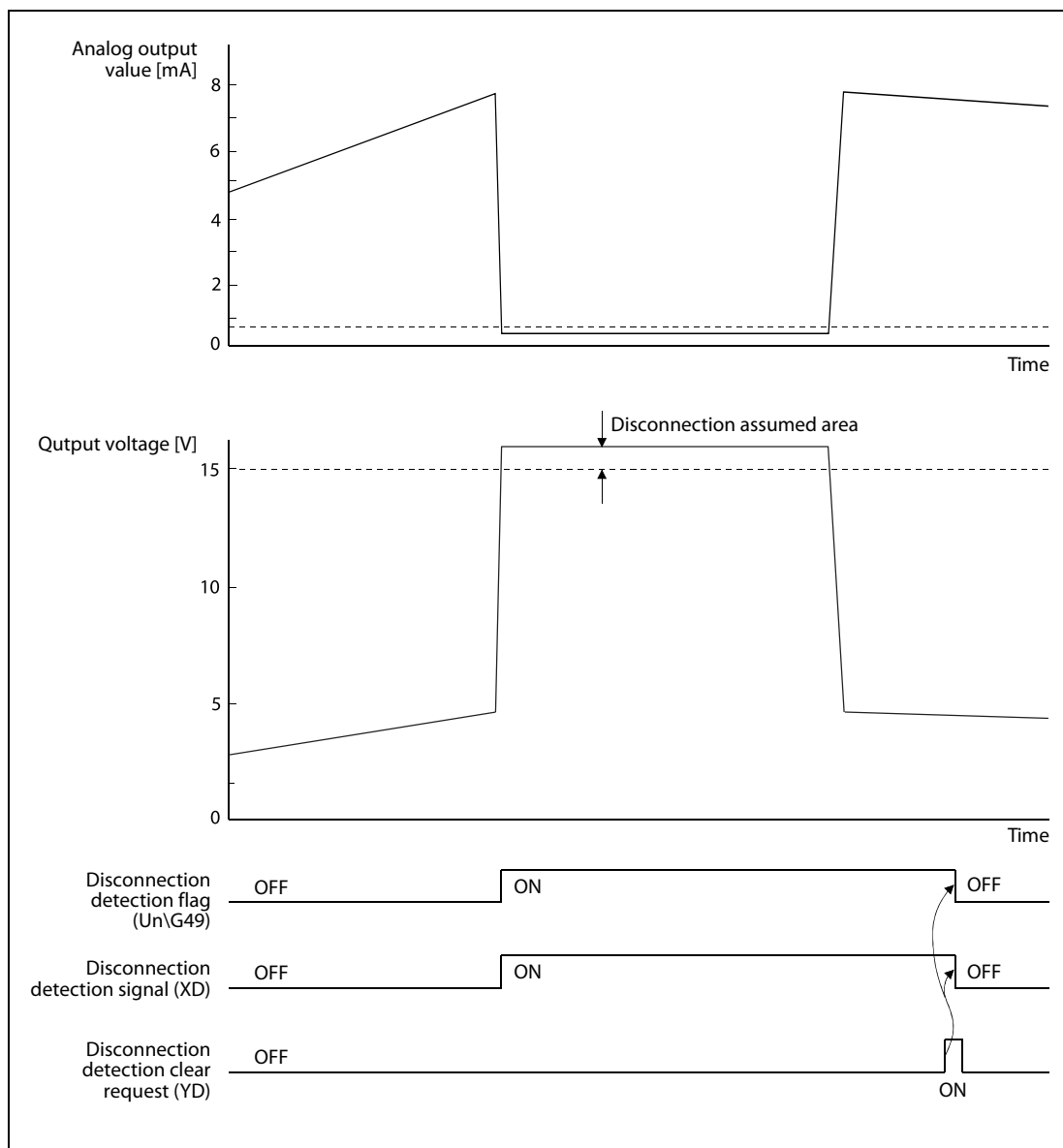


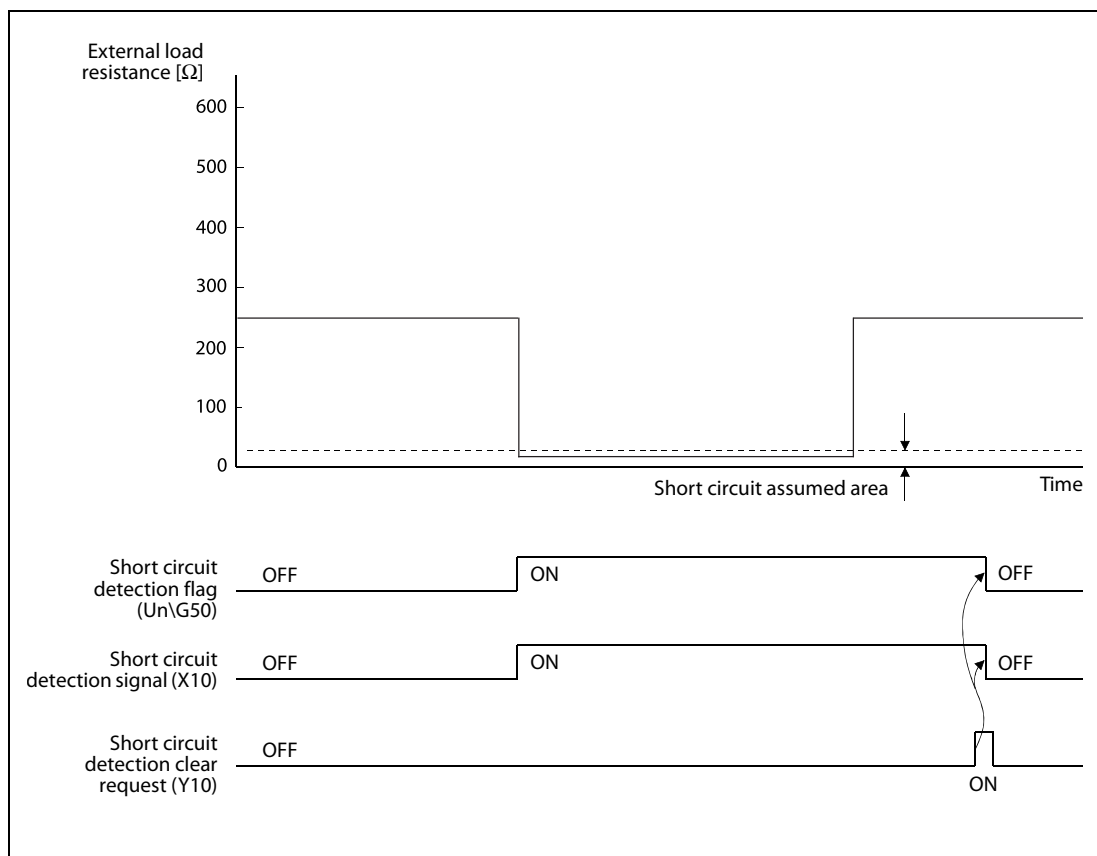
Fig. 3-8: When the output voltage is 15 V or more, a disconnection is assumed

### 3.3.7 Short circuit detection function

When the external load resistance falls to 30 Ω or less while an output current of 4 mA or more is set, a short circuit is detected and both the short circuit detection flag (buffer memory address Un\G50) and short circuit detection signal (X10) turn ON. In addition, the ALM LED is switched on to indicate the short circuit. A short circuit is detected only on an output enabled channel.

The short circuit detection flag (buffer memory address Un\G50) and short circuit detection signal (X10) turn OFF when the operating condition setting request (Y9) or short circuit detection clear request (Y10) turns ON.

For each channel, the short circuit detection function can be enabled or disabled by the short circuit detection setting (buffer memory address Un\G45). To enable the short circuit detection, write "0" to the bit position corresponding to the channel number and turn ON the operating condition setting request (Y9). Short circuit detection is disabled for all channels as a default.



**Fig. 3-9:** With an external load of 30 Ω or less, a short circuit is assumed

**NOTE**

If the ground connections of 2 or more actuators are connected with each other at the actuators side, a short circuit may be not detected for these channels. In such a case, disable the short circuit detection.

### 3.3.8 HART Master Function

#### What is HART?

HART stands for **H**ighway **A**dressable **R**emote **T**ransducer.

HART Communication is a bi-directional industrial field communication protocol used to communicate between intelligent field instruments and host systems. A host system can be a handheld device, a Distributed Control System, Asset Management System, Safety System or a PLC.

There are several reasons to have a host communicate with a field instrument. These include:

- Device Configuration or re-configuration
- Device Diagnostics
- Device Troubleshooting
- Reading the values of additional measurements provided by the device
- Device Health and Status
- And much more!

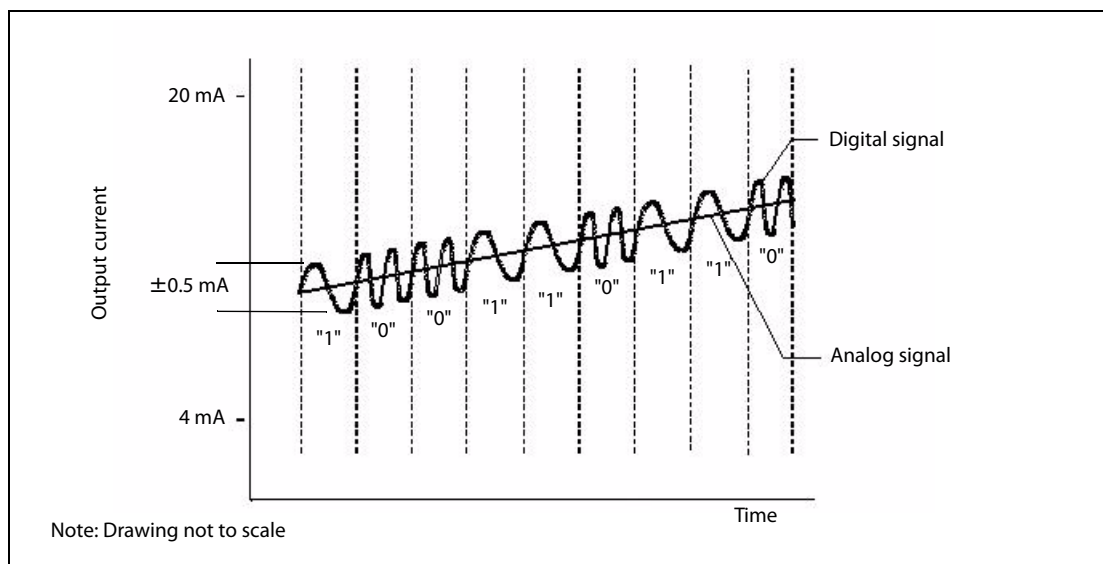
#### How HART Works

When using the ME1DA6HAI-Q, HART communication takes place between the analog output module and a HART-enabled field device, for example an actuator for a valve. The ME1DA6HAI-Q can communicate with up to six HART-enabled devices. (One HART device connected to each channel.)

Communication occurs using standard instrumentation grade wire and using standard wiring and termination practices – no additional wiring is required.

HART provides two simultaneous communication channels: the 4 to 20 mA analog signal and a digital signal. The 4 to 20 mA signal communicates the analog output value fast, robust and reliable. Additional device information is communicated using a digital signal that is superimposed on the analog signal. The digital signal contains information from the device including device status, diagnostics, etc.

The HART protocol makes use of the Bell 202 Frequency Shift Keying (FSK) standard to superimpose digital communication signals at a low level on top of the 4 to 20 mA analog signal.



**Fig. 3-10:** Digital communication is superimposed on the analog signal

A digital signal with a frequency of 2200 Hz is interpreted as logical "0", whereas a frequency of 1200 Hz is interpreted as logical "1".

The HART protocol communicates without interrupting the 4 to 20 mA signal and allows a host appli-



cation (in this case the ME1DA6HAI-Q) to get two or more digital updates per second from a field device. As the digital FSK signal is phase continuous, there is no interference with the analog 4 to 20 mA signal.

HART is a master/slave protocol which means that a field (slave) device only speaks when spoken to by the ME1DA6HAI-Q (master). This is done by commands send by the ME1DA6HAI-Q. Codes vary by manufacturer/device.

Examples for commands:

- Set Primary Variable Units
- Set Upper Range
- Set Lower Range
- Set Damping Value
- Set Tag
- Set Date
- Set Descriptor
- Perform Loop Test - Force loop current to specific value
- Initiate Self Test - Start device self test
- Get More Status Available Information

**NOTE**

The supported commands are depended on the specification of the HART transmitter.

The ME1DA6HAI-Q can operate as a HART master with protocol revision 6.

**NOTE**

The start up time of the connected HART devices must be considered. If it is long, HART communication errors may occur after switching on the system.

**HART Data**

The following list is only a brief overview of the data transmitted via the HART protocol. Fore more information please refer to the description of the buffer memory (Section 3.5.1).

- Digital data: 35 to 40 valuable data items standard in every HART device
- Device identification: device tag, supplier, device type and revision, device serial number
- Calibration data: upper and lower range values, upper and lower sensor limits, PV damping, last calibration date
- Process variables: primary variable plus secondary measurements and multivariable parameters
- Status/diagnostic alerts: device malfunction, configuration change, power fail restart, loop current fixed or saturated, primary or secondary variable out of limits, communication error etc.

**More information**

This short overview about the HART protocol is only a extract of the information provided on the website of the HART Communication Foundation. You can find much more information about HART and answers to frequently asked questions on their website at [www.hartcomm2.org](http://www.hartcomm2.org).

**FDT/DTM function support**

Using a commercially available FDT, reading/writing the HART transmitter's parameters and monitoring the HART transmitter status are executable via the ME1DA6HAI-Q.

Refer to section 4.6 (Setting of the HART Devices) for more details about the FDT/DTM\* system structure.

\* FDT stands for **F**ield **D**evice **T**ool and DTM stands for **D**evice **T**ype **M**anager. FDT/DTM is a communication technique for the manufacturer-independent configuration of processing systems at a field bus.

## 3.4 I/O Signals for the Programmable Controller CPU

### 3.4.1 List of I/O signals

Note that I/O numbers (X/Y) shown in this section and thereafter are the values when the start I/O number for the ME1DA6HAI-Q is set to 0 (i.e. the module is mounted to the I/O slot 0 of the main base unit).

Signal direction CPU Module ← ME1DA6HAI-Q		Signal direction CPU Module → ME1DA6HAI-Q	
Device No. (Input)	Signal name	Device No. (Output)	Signal name
X0	Module ready	Y0	Use prohibited
X1	Use prohibited	Y1	CH1 Output enable/disable flag
X2		Y2	CH2 Output enable/disable flag
X3		Y3	CH3 Output enable/disable flag
X4		Y4	CH4 Output enable/disable flag
X5		Y5	CH5 Output enable/disable flag
X6		Y6	CH6 Output enable/disable flag
X7		Y7	Use prohibited
X8		Y8	
X9	Operating condition setting completed flag	Y9	Operating condition setting request
XA	Use prohibited	YA	Use prohibited
XB		YB	
XC		YC	
XD	Disconnection detection signal	YD	Disconnection detection clear request
XE	Warning output signal	YE	Warning output clear request
XF	Error flag	YF	Error clear request
X10	Short circuit detection signal	Y10	Short circuit detection clear request
X11 to X1F	Use prohibited	Y11 to Y1F	Use prohibited

**Tab. 3-9:** I/O signals of the ME1DA6HAI-Q

#### NOTE

The "Use prohibited" signals cannot be used by the user since they are for system use only. If these are turned ON/OFF by the sequence program, the performance of the HART analog output module cannot be guaranteed.

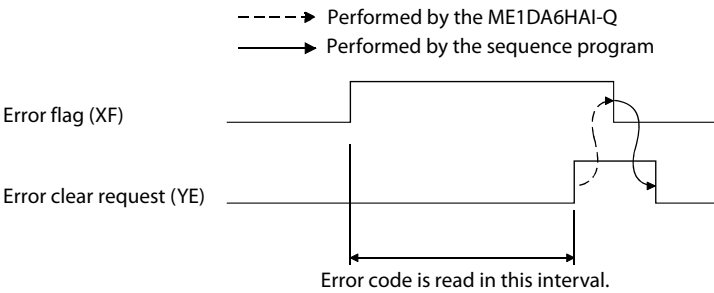
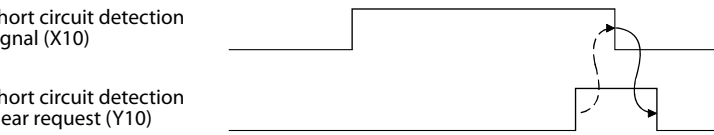
### 3.4.2 Details of I/O signals

#### Input signals

Device No.	Signal Name	Description
X0	Module ready	<ul style="list-style-type: none"> <li>When the programmable controller CPU is powered on or reset, this signal turns on once the preparation for D/A conversion has been completed. Afterwards D/A conversion processing is performed.</li> <li>When the analog output module has a watchdog timer error*, "Module ready" (X0) turns OFF (In this case D/A conversion processing is not performed.)</li> </ul>
X9	Operating condition setting completed flag	<ul style="list-style-type: none"> <li>This signal is used as an interlock condition to turn ON/OFF the Operating condition setting request (Y9) when any of the following settings has been changed.                             <ul style="list-style-type: none"> <li>Short-circuit detection setting (buffer memory address Un\G45)</li> <li>Rate control enable/disable setting (buffer memory address Un\G46)</li> <li>Disconnection detection/warning output setting (buffer memory address Un\G47)</li> <li>Scaling function setting (buffer memory address Un\G53)</li> <li>Increase/decrease digital limit value (buffer memory addresses Un\G70 to 81)</li> </ul> </li> <li>The operating condition setting completed flag (X9) turns OFF when the operating condition setting request (Y9) is ON.</li> </ul> <div style="text-align: right; margin-right: 20px;"> <p>-----&gt; Performed by the ME1DA6HAI-Q</p> <p>—————&gt; Performed by the sequence program</p> </div> <p><b>NOTE</b> If the "Intelligent function utility" is used for configuration, the settings made with this function are restored under the following conditions:</p> <ul style="list-style-type: none"> <li>CPU Power off → CPU RUN</li> <li>CPU RESET → CPU RUN</li> <li>CPU STOP → CPU RUN</li> </ul>
XD	Disconnection detection signal	<ul style="list-style-type: none"> <li>This input turns ON if a disconnection is detected on any channel.</li> <li>Turning ON the disconnection detection clear request (YD) or operating condition setting request (Y9) turns OFF the disconnection detection signal (XD).</li> </ul> <div style="text-align: right; margin-right: 20px;"> <p>-----&gt; Performed by the ME1DA6HAI-Q</p> <p>—————&gt; Performed by the sequence program</p> </div>
XE	Warning output signal	<ul style="list-style-type: none"> <li>This signal turns ON if the digital input value on any of the channels enabled for D/A conversion rises to or above the warning output upper limit value or falls below the warning output lower limit value.</li> <li>Turning ON the warning output clear request (YE) or operating condition setting request (Y9) turns OFF the warning output signal (XE).</li> </ul> <div style="text-align: right; margin-right: 20px;"> <p>-----&gt; Performed by the ME1DA6HAI-Q</p> <p>—————&gt; Performed by the sequence program</p> </div>

**Tab. 3-10:** Detailed description of the input signals (Signal direction ME1DA6HAI-Q → CPU Module)

\* When a watchdog timer error occurs, the RUN LED of the analog output module turns off.

Device No.	Signal Name	Description
XF	Error flag	<ul style="list-style-type: none"> <li>The error flag turns ON when a write error occurs</li> <li>To turn the error flag (XF) OFF, remove the cause of the error and set the error clear request (YF) to ON.</li> </ul> <p>The error code (buffer memory address Un\G19) changes to 0 and the ERR. LED turns off.</p> <p>                     -----&gt; Performed by the ME1DA6HAI-Q                      —————&gt; Performed by the sequence program                 </p>  <p>Error code is read in this interval.</p>
X10	Short circuit detection signal	<ul style="list-style-type: none"> <li>This signal turns ON if a short circuit is detected on any channel.</li> <li>Turning ON the short circuit detection clear request (Y10) or operating condition setting request (Y9) turns OFF the short circuit detection signal (X10).</li> </ul> <p>                     -----&gt; Performed by the ME1DA6HAI-Q                      —————&gt; Performed by the sequence program                 </p> 

**Tab. 3-11:** Detailed description of the input signals (Signal direction ME1DA6HAI-Q → CPU Module)

**Output signals**

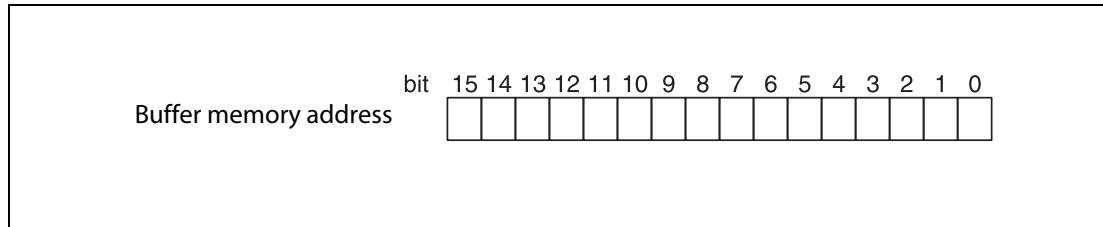
Device No.	Signal Name	Description
Y1 to Y6	CH□ output enable/disable flag	<ul style="list-style-type: none"> <li>Specifies whether to output the D/A converted value or offset value for each channel. <ul style="list-style-type: none"> <li>ON: D/A converted value</li> <li>OFF: Offset value</li> </ul> </li> <li>The D/A conversion speed is constant regardless of whether the output enable/disable flag is ON or OFF.</li> </ul>
Y9	Operating condition setting request	<ul style="list-style-type: none"> <li>Turn ON this signal when changing any of the following settings to make the settings valid. <ul style="list-style-type: none"> <li>Short-circuit detection setting (buffer memory address Un\G45)</li> <li>Rate control enable/disable setting (buffer memory address Un\G46)</li> <li>Disconnection detection/warning output setting (buffer memory address Un\G47)</li> <li>Scaling function setting (buffer memory address Un\G53)</li> <li>Increase/decrease digital limit value (buffer memory addresses Un\G70 to 81)</li> </ul> </li> <li>For the ON/OFF timing, please refer to the entry for input X9 in table 3-10.</li> </ul>
YD	Disconnection detection clear request	<ul style="list-style-type: none"> <li>Turn ON this signal to clear the disconnection detection.</li> <li>For the ON/OFF timing, please refer to the entry for input XD in table 3-10.</li> </ul>
YE	Warning output clear request	<ul style="list-style-type: none"> <li>Turn ON this signal to clear the warning output.</li> <li>For the ON/OFF timing, please refer to the entry for input XE in table 3-10.</li> </ul>
YF	Error clear request	<ul style="list-style-type: none"> <li>Turn this signal ON to clear a write error.</li> <li>For the ON/OFF timing, please refer to the entry for input XF in table 3-11.</li> </ul>
Y10	Short circuit detection clear request	<ul style="list-style-type: none"> <li>Turn ON this signal to clear the short circuit detection.</li> <li>For the ON/OFF timing, please refer to the entry for input X10 in table 3-11.</li> </ul>

**Tab. 3-12:** Detailed description of the output signals (Signal direction CPU Module → ME1DA6HAI-Q)

## 3.5 Buffer Memory

The HART analog output module has a memory range assigned as a buffer for temporary storage of data, such as digital values intended for D/A conversion or HART device data. The PLC CPU can access this buffer and both read the stored values from it and write new values to it which the module can then process (digital values, settings for the module's functions etc).

Each buffer memory address consists of 16 bits.



**Fig. 3-11:** Assignments of bits to a buffer memory address

### NOTE

Do not write data in the "system areas" of the buffer memory. If data is written to any of the system areas, the PLC system may not be operated properly. Some of the user areas contain partially system areas. Care must be taken when reading/writing to the buffer memory.

Also, do not write data (e.g. in a sequence program) to the buffer memory area where writing is disabled. Doing so may cause malfunction.

The "Default" value indicated in the following tables is the initial value set after the power is turned on or the PLC CPU is reset.

### Instructions for data exchange with the buffer memory

Communication between the PLC CPU and the buffer memory of special function modules is performed with FROM and TO instructions.

The buffer memory of a special function module can also be accessed directly, e. g. with a MOV instruction. The special function module addressed in this way can be mounted on a base unit or an extension base unit but not in remote I/O stations.

Format of the device address: Un\Gn

- Un: Head address of the special function module
- Gn: Buffer memory address (decimal)

For example the device address U3\G11 designates the buffer memory address 11 in the special function module with the head address 3 (X/Y30 to X/Y3F).

In this User's Manual the latter form of addressing is used throughout.

For full documentation of all the instructions with examples please refer to the Programming Manual for the A/Q series and the MELSEC System Q, art. no. 87431.

### 3.5.1 Buffer memory assignment

Address		Description	Default	R/W*	Reference
Hexa-decimal	Decimal				
0H	0	System area	—	—	—
1H	1	CH1	0	R/W	Section 3.5.2
2H	2	CH2			
3H	3	CH3			
4H	4	CH4			
5H	5	CH5			
6H	6	CH6			
7H	7	System area	—	—	—
8H	8				
9H	9				
AH	10				
BH	11	CH1	0	R	Section 3.5.3
CH	12	CH2			
DH	13	CH3			
EH	14	CH4			
FH	15	CH5			
10H	16	CH6			
11H	17	System area	—	—	—
12H	18				
13H	19	Error code	0	R	Section 3.5.4
14H	20	Setting range (CH1 to CH4)	0000H	R	Section 3.5.5
15H	21	Setting range (CH5 and CH6)			
16H	22	System area	—	—	—
to	to				
2CH	44				
2DH	45	Short circuit detection setting	003FH	R/W	Section 3.5.6
2EH	46	Rate control enable/disable setting	003FH	R/W	Section 3.5.7
2FH	47	Disconnection detection setting & Warning output setting	3F3FH	R/W	Section 3.5.8
30H	48	Warning output flag	0	R	Section 3.5.9
31H	49	Disconnection detection flag	0	R	Section 3.5.10
32H	50	Short circuit detection flag	0	R	Section 3.5.11
33H	51	System area	—	—	—
34H	52				

**Tab. 3-13:** Buffer memory assignment of the ME1DA6HAI-Q (1/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

Address		Description			Default	R/W*	Reference
Hexa-decimal	Decimal						
35H	53	Scaling enable/disable setting			003FH	R/W	Section 3.5.12
36H	54	CH1	Scaling	Lower limit value	0	R/W	Section 3.5.13
37H	55			Upper limit value			
38H	56	CH2	Scaling	Lower limit value			
39H	57			Upper limit value			
3AH	58	CH3	Scaling	Lower limit value			
3BH	59			Upper limit value			
3CH	60	CH4	Scaling	Lower limit value			
3DH	61			Upper limit value			
3EH	62	CH5	Scaling	Lower limit value			
3FH	63			Upper limit value			
40H	64	CH6	Scaling	Lower limit value			
41H	65			Upper limit value			
42H	66	System area			—	—	—
to	to						
45H	69						
46H	70	CH1	Rate control	Increase digital limit value	32000	R/W	Section 3.5.14
47H	71			Decrease digital limit value			
48H	72	CH2	Rate control	Increase digital limit value	32000		
49H	73			Decrease digital limit value			
4AH	74	CH3	Rate control	Increase digital limit value	32000		
4BH	75			Decrease digital limit value			
4CH	76	CH4	Rate control	Increase digital limit value	32000		
4DH	77			Decrease digital limit value			
4EH	78	CH5	Rate control	Increase digital limit value	32000		
4FH	79			Decrease digital limit value			
50H	80	CH6	Rate control	Increase digital limit value	32000		
51H	81			Decrease digital limit value			
52H	82	System area			—	—	—
to	to						
55H	85						
56H	86	CH1	Warning output	Upper limit value	0	R/W	Section 3.5.15
57H	87			Lower limit value			
58H	88	CH2	Warning output	Upper limit value	0		
59H	89			Lower limit value			
5AH	90	CH3	Warning output	Upper limit value	0		
5BH	91			Lower limit value			
5CH	92	CH4	Warning output	Upper limit value	0		
5DH	93			Lower limit value			
5EH	94	CH5	Warning output	Upper limit value	0		
5FH	95			Lower limit value			
60H	96	CH6	Warning output	Upper limit value	0		
61H	97			Lower limit value			
62H	98	System area			—	—	—
to	to						
9FH	159						

**Tab. 3-14:** Buffer memory assignment of the ME1DA6HAI-Q (2/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled



Address		Description	Default	R/W*	Reference			
Hexa-decimal	Decimal							
A0H	160	HART	CH1 to CH6 enable	0000H	R/W	Section 3.5.16		
A1H	161		Scan list	0000H	R	Section 3.5.17		
A2H	162		Current cycle time	0	R	Section 3.5.18		
A3H	163		Maximum cycle time	0	R			
A4H	164		Minimum cycle time	0	R			
A5H	165	System area	—	—	—			
to	to		—	—	—			
AFH	175		—	—	—			
B0H	176	CH1	HART maximum retries	3	R/W	Section 3.5.19		
B1H	177	CH2						
B2H	178	CH3						
B3H	179	CH4						
B4H	180	CH5						
B5H	181	CH6						
B6H	182	System area	—	—	—			
to	to		—	—	—			
BEH	190		—	—	—			
BFH	191	HART device information refresh interval [seconds]		30	R/W	Section 3.5.20		
C0H	192	System area	—	—	—			
to	to		—	—	—			
EFH	239		—	—	—			
F0H	240	CH1	HART field device status		0000H	R	Section 3.5.21	
F1H	241		HART extended field device status		0000H	R	Section 3.5.22	
F2H	242		HART device variable status	Primary value (PV), secondary value (SV)		0000H	R	Section 3.5.23
F3H	243			Tertiary value (TV), fourth value (FV)		0000H	R	
F4H	244		Process variable	Primary value (PV)	Low word	0000H	R	Section 3.5.24
F5H	245				High word	7FC0H		
F6H	246			Secondary value (SV)	Low word	0000H	R	
F7H	247				High word	7FC0H		
F8H	248			Tertiary value (TV)	Low word	0000H	R	
F9H	249				High word	7FC0H		
FAH	250			Fourth value (FV)	Low word	0000H	R	
FBH	251				High word	7FC0H		

**Tab. 3-15:** Buffer memory assignment of the ME1DA6HAI-Q (3/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

Address		Description	Default	R/W*	Reference			
Hexa-decimal	Decimal							
FC <sub>H</sub>	252	CH2	HART field device status		0000 <sub>H</sub>	R	Section 3.5.21	
FD <sub>H</sub>	253		HART extended field device status		0000 <sub>H</sub>	R	Section 3.5.22	
FE <sub>H</sub>	254		HART device variable status	Primary value (PV), secondary value (SV)		0000 <sub>H</sub>	R	Section 3.5.23
FF <sub>H</sub>	255			Tertiary value (TV), fourth value (FV)		0000 <sub>H</sub>	R	
100 <sub>H</sub>	256		Process variable	Primary value (PV)	Low word	0000 <sub>H</sub>	R	Section 3.5.24
101 <sub>H</sub>	257				High word	7FC0 <sub>H</sub>		
102 <sub>H</sub>	258			Secondary value (SV)	Low word	0000 <sub>H</sub>	R	
103 <sub>H</sub>	259				High word	7FC0 <sub>H</sub>		
104 <sub>H</sub>	260			Tertiary value (TV)	Low word	0000 <sub>H</sub>	R	
105 <sub>H</sub>	261				High word	7FC0 <sub>H</sub>		
106 <sub>H</sub>	262			Fourth value (FV)	Low word	0000 <sub>H</sub>	R	
107 <sub>H</sub>	263				High word	7FC0 <sub>H</sub>		
108 <sub>H</sub>	264		CH3	HART field device status		0000 <sub>H</sub>	R	Section 3.5.21
109 <sub>H</sub>	265			HART extended field device status		0000 <sub>H</sub>	R	Section 3.5.22
10A <sub>H</sub>	266	HART device variable status		Primary value (PV), secondary value (SV)		0000 <sub>H</sub>	R	Section 3.5.23
10B <sub>H</sub>	267			Tertiary value (TV), fourth value (FV)		0000 <sub>H</sub>	R	
10C <sub>H</sub>	268	Process variable		Primary value (PV)	Low word	0000 <sub>H</sub>	R	Section 3.5.24
10D <sub>H</sub>	269				High word	7FC0 <sub>H</sub>		
10E <sub>H</sub>	270			Secondary value (SV)	Low word	0000 <sub>H</sub>	R	
10F <sub>H</sub>	271				High word	7FC0 <sub>H</sub>		
110 <sub>H</sub>	272			Tertiary value (TV)	Low word	0000 <sub>H</sub>	R	
111 <sub>H</sub>	273				High word	7FC0 <sub>H</sub>		
112 <sub>H</sub>	274			Fourth value (FV)	Low word	0000 <sub>H</sub>	R	
113 <sub>H</sub>	275				High word	7FC0 <sub>H</sub>		
114 <sub>H</sub>	276	CH4		HART field device status		0000 <sub>H</sub>	R	Section 3.5.21
115 <sub>H</sub>	277			HART extended field device status		0000 <sub>H</sub>	R	Section 3.5.22
116 <sub>H</sub>	278		HART device variable status	Primary value (PV), secondary value (SV)		0000 <sub>H</sub>	R	Section 3.5.23
117 <sub>H</sub>	279			Tertiary value (TV), fourth value (FV)		0000 <sub>H</sub>	R	
118 <sub>H</sub>	280		Process variable	Primary value (PV)	Low word	0000 <sub>H</sub>	R	Section 3.5.24
119 <sub>H</sub>	281				High word	7FC0 <sub>H</sub>		
11A <sub>H</sub>	282			Secondary value (SV)	Low word	0000 <sub>H</sub>	R	
11B <sub>H</sub>	283				High word	7FC0 <sub>H</sub>		
11C <sub>H</sub>	284			Tertiary value (TV)	Low word	0000 <sub>H</sub>	R	
11D <sub>H</sub>	285				High word	7FC0 <sub>H</sub>		
11E <sub>H</sub>	286			Fourth value (FV)	Low word	0000 <sub>H</sub>	R	
11F <sub>H</sub>	287				High word	7FC0 <sub>H</sub>		

**Tab. 3-16:** Buffer memory assignment of the ME1DA6HAI-Q (4/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

Address		Description	Default	R/W*	Reference			
Hexa-decimal	Decimal							
120H	288	CH5	HART field device status		0000H	R	Section 3.5.21	
121H	289		HART extended field device status		0000H	R	Section 3.5.22	
122H	290		HART device variable status	Primary value (PV), secondary value (SV)		0000H	R	Section 3.5.23
123H	291			Tertiary value (TV), fourth value (FV)		0000H	R	
124H	292		Process variable	Primary value (PV)	Low word	0000H	R	Section 3.5.24
125H	293				High word	7FC0H		
126H	294			Secondary value (SV)	Low word	0000H	R	
127H	295				High word	7FC0H		
128H	296			Tertiary value (TV)	Low word	0000H	R	
129H	297				High word	7FC0H		
12AH	298			Fourth value (FV)	Low word	0000H	R	
12BH	299				High word	7FC0H		
12CH	300		CH6	HART field device status		0000H	R	Section 3.5.21
12DH	301	HART extended field device status		0000H	R	Section 3.5.22		
12EH	302	HART device variable status		Primary value (PV), secondary value (SV)		0000H	R	Section 3.5.23
12FH	303			Tertiary value (TV), fourth value (FV)		0000H	R	
130H	304	Process variable		Primary value (PV)	Low word	0000H	R	Section 3.5.24
131H	305				High word	7FC0H		
132H	306			Secondary value (SV)	Low word	0000H	R	
133H	307				High word	7FC0H		
134H	308			Tertiary value (TV)	Low word	0000H	R	
135H	309				High word	7FC0H		
136H	310			Fourth value (FV)	Low word	0000H	R	
137H	311				High word	7FC0H		
138H	312	System area		—	—	—		
to	to							
15FH	351							
160H	352	HART Command (Request)	Request flag		0	R/W	Section 3.5.25	
161H	353		Channel		0000H			
162H	354		Code		0000H			
163H	355		Data size		0			
164H	356		Data to be sent		0	R/W		
to	to							
1E3H	483	System area		—	—	—		
1E4H	484							
to	to							
1EFH	495	HART Command (Answer)		Answer flag		0000H	R	Section 3.5.26
1F0H	496			Channel		0000H		
1F1H	497			Code		0000H		
1F2H	498			Data size		0		
1F3H	499			Received data		0	R	
to	to							
273H	627							

**Tab. 3-17:** Buffer memory assignment of the ME1DA6HAI-Q (5/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
 R : Read enabled  
 W : Write enabled

Address		Description	Default	R/W*	Reference
Hexa-decimal	Decimal				
274 <sub>H</sub>	628	System area	—	—	—
to	to				
37F <sub>H</sub>	895				
380 <sub>H</sub>	896	CH1 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27
to	to			Tag	
383 <sub>H</sub>	899			Message	
384 <sub>H</sub>	900			Descriptor	
to	to			Manufacturer ID / Expanded manufacturer ID (HART 7)	
393 <sub>H</sub>	915			Device Type / Expanded device type (HART 7)	
394 <sub>H</sub>	916			Device ID	
to	to			Revisions	
39B <sub>H</sub>	923			Device function flags	
39C <sub>H</sub>	924			Long tag	
39D <sub>H</sub>	925			Private label distributor code (HART 7)	
39E <sub>H</sub>	926			Device profile (HART 7)	
39F <sub>H</sub>	927				
3A0 <sub>H</sub>	928				
3A1 <sub>H</sub>	929				
3A2 <sub>H</sub>	930				
3A3 <sub>H</sub>	931				
to	to				
3B2 <sub>H</sub>	946				
3B3 <sub>H</sub>	947				
3B4 <sub>H</sub>	948				
3B5 <sub>H</sub>	949	System area	—	—	—
3B6 <sub>H</sub>	950	CH1 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27
3B7 <sub>H</sub>	951			Final assembly number	
3B8 <sub>H</sub>	952			Date	
3B9 <sub>H</sub>	953			Write Protect	
3BA <sub>H</sub>	954			PV range unit code	
3BB <sub>H</sub>	955			PV Upper range value	
3BC <sub>H</sub>	956			PV Lower range value	
3BD <sub>H</sub>	957			PV Damping value	
3BE <sub>H</sub>	958			Transfer function	
3BF <sub>H</sub>	959			PV Unit code	
3C0 <sub>H</sub>	960			SV Unit code	
3C1 <sub>H</sub>	961			TV Unit code	
3C2 <sub>H</sub>	962			FV Unit code	
3C3 <sub>H</sub>	963				
3C4 <sub>H</sub>	964				
3C5 <sub>H</sub>	965				
3C6 <sub>H</sub>	966				
3C7 <sub>H</sub>	967	System area	—	—	—

**Tab. 3-18:** Buffer memory assignment of the ME1DA6HAI-Q (6/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

Address		Description	Default	R/W*	Reference	
Hexa-decimal	Decimal					
3C8 <sub>H</sub>	968	CH2 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27	
to	to					Tag
3CB <sub>H</sub>	971					Message
3CC <sub>H</sub>	972					
to	to					Descriptor
3DB <sub>H</sub>	987					
3DC <sub>H</sub>	988					
to	to					Manufacturer ID / Expanded manufacturer ID (HART 7)
3E3 <sub>H</sub>	995					
3E4 <sub>H</sub>	996					Device Type / Expanded device type (HART 7)
3E5 <sub>H</sub>	997					
3E6 <sub>H</sub>	998					Device ID
3E7 <sub>H</sub>	999					
3E8 <sub>H</sub>	1000					Revisions
3E9 <sub>H</sub>	1001					
3EA <sub>H</sub>	1002					Device function flags
3EB <sub>H</sub>	1003					
to	to	Long tag				
3FA <sub>H</sub>	1018					
3FB <sub>H</sub>	1019	Private label distributor code (HART 7)				
3FC <sub>H</sub>	1020					
3FD <sub>H</sub>	1021	System area	—	—	—	
3FE <sub>H</sub>	1022	CH2 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27	
3FF <sub>H</sub>	1023					Final assembly number
400 <sub>H</sub>	1024					Date
401 <sub>H</sub>	1025					
402 <sub>H</sub>	1026					Write Protect
403 <sub>H</sub>	1027					PV range unit code
404 <sub>H</sub>	1028					PV Upper range value
405 <sub>H</sub>	1029					
406 <sub>H</sub>	1030					PV Lower range value
407 <sub>H</sub>	1031					PV Damping value
408 <sub>H</sub>	1032					
409 <sub>H</sub>	1033					Transfer function
40A <sub>H</sub>	1034					
40B <sub>H</sub>	1035					PV Unit code
40C <sub>H</sub>	1036	SV Unit code				
40D <sub>H</sub>	1037	TV Unit code				
40E <sub>H</sub>	1038	FV Unit code				
40F <sub>H</sub>	1039	System area	—	—	—	

**Tab. 3-19:** Buffer memory assignment of the ME1DA6HAI-Q (7/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

Address		Description	Default	R/W*	Reference	
Hexa-decimal	Decimal					
410 <sub>H</sub>	1040	CH3 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27	
to	to					Tag
413 <sub>H</sub>	1043					Message
414 <sub>H</sub>	1044					
to	to					Descriptor
423 <sub>H</sub>	1059					
424 <sub>H</sub>	1060					Manufacturer ID / Expanded manufacturer ID (HART 7)
to	to					
42B <sub>H</sub>	1067					Device Type / Expanded device type (HART 7)
42C <sub>H</sub>	1068					
42D <sub>H</sub>	1069					Device ID
42E <sub>H</sub>	1070					
42F <sub>H</sub>	1071					Revisions
430 <sub>H</sub>	1072					
431 <sub>H</sub>	1073					Device function flags
432 <sub>H</sub>	1074					
433 <sub>H</sub>	1075	Long tag				
to	to					
442 <sub>H</sub>	1090	Private label distributor code (HART 7)				
443 <sub>H</sub>	1091					
444 <sub>H</sub>	1092	Device profile (HART 7)				
445 <sub>H</sub>	1093	System area	—	—	—	
446 <sub>H</sub>	1094	CH3 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27	
447 <sub>H</sub>	1095					Final assembly number
448 <sub>H</sub>	1096					Date
449 <sub>H</sub>	1097					Write Protect
44A <sub>H</sub>	1098					PV range unit code
44B <sub>H</sub>	1099					PV Upper range value
44C <sub>H</sub>	1100					PV Lower range value
44D <sub>H</sub>	1101					PV Damping value
44E <sub>H</sub>	1102					Transfer function
44F <sub>H</sub>	1103					PV Unit code
450 <sub>H</sub>	1104					SV Unit code
451 <sub>H</sub>	1105					TV Unit code
452 <sub>H</sub>	1106					FV Unit code
453 <sub>H</sub>	1107					
454 <sub>H</sub>	1108					
455 <sub>H</sub>	1109					
456 <sub>H</sub>	1110					
457 <sub>H</sub>	1111	System area	—	—	—	

**Tab. 3-20:** Buffer memory assignment of the ME1DA6HAI-Q (8/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

Address		Description	Default	R/W*	Reference		
Hexa-decimal	Decimal						
458 <sub>H</sub>	1112	CH4 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27		
to	to					Tag	
45B <sub>H</sub>	1115					Message	
45C <sub>H</sub>	1116						
to	to					Descriptor	
46B <sub>H</sub>	1131						
46C <sub>H</sub>	1132						
to	to					Manufacturer ID / Expanded manufacturer ID (HART 7)	
473 <sub>H</sub>	1139						
474 <sub>H</sub>	1140					Device Type / Expanded device type (HART 7)	
475 <sub>H</sub>	1141						
476 <sub>H</sub>	1142						Device ID
477 <sub>H</sub>	1143						
478 <sub>H</sub>	1144						Revisions
479 <sub>H</sub>	1145						
47A <sub>H</sub>	1146						Device function flags
47B <sub>H</sub>	1147						
to	to	Long tag					
48A <sub>H</sub>	1162						
48B <sub>H</sub>	1163	Private label distributor code (HART 7)					
48C <sub>H</sub>	1164						
48D <sub>H</sub>	1165	System area	—	—	—		
48E <sub>H</sub>	1166	CH4 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27		
48F <sub>H</sub>	1167					Final assembly number	
490 <sub>H</sub>	1168					Date	
491 <sub>H</sub>	1169					Write Protect	
492 <sub>H</sub>	1170					PV range unit code	
493 <sub>H</sub>	1171					PV Upper range value	
494 <sub>H</sub>	1172						
495 <sub>H</sub>	1173					PV Lower range value	
496 <sub>H</sub>	1174						
497 <sub>H</sub>	1175					PV Damping value	
498 <sub>H</sub>	1176						
499 <sub>H</sub>	1177					Transfer function	
49A <sub>H</sub>	1178						
49B <sub>H</sub>	1179	PV Unit code					
49C <sub>H</sub>	1180	SV Unit code					
49D <sub>H</sub>	1181	TV Unit code					
49E <sub>H</sub>	1182	FV Unit code					
49F <sub>H</sub>	1183	System area	—	—	—		

**Tab. 3-21:** Buffer memory assignment of the ME1DA6HAI-Q (9/11)

Indicates whether reading from and writing to a sequence program are enabled.

R : Read enabled

W : Write enabled

Address		Description	Default	R/W*	Reference	
Hexa-decimal	Decimal					
4A0H	1184	CH5 Information about HART device	0000H	R	Section 3.5.27	
to	to					Tag
4A3H	1187					Message
4A4H	1188					
to	to					Descriptor
4B3H	1203					
4B4H	1204					Manufacturer ID / Expanded manufacturer ID (HART 7)
to	to					
4BBH	1211					Device Type / Expanded device type (HART 7)
4BCH	1212					
4BDH	1213					Device ID
4BEH	1214					
4BFH	1215					Revisions
4C0H	1216					
4C1H	1217					Device function flags
4C2	1218					
4C3H	1219					Long tag
to	to					
4D2H	1234	Private label distributor code (HART 7)				
4D3H	1235					
4D4H	1236	Device profile (HART 7)				
4D5H	1237	System area	—	—	—	
4D6H	1238	CH5 Information about HART device	0000H	R	Section 3.5.27	
4D7H	1239					Final assembly number
4D8H	1240					Date
4D9H	1241					Write Protect
4DAH	1242					PV range unit code
4DBH	1243					PV Upper range value
4DCH	1244					PV Lower range value
4DDH	1245					PV Damping value
4DEH	1246					Transfer function
4DFH	1247					PV Unit code
4E0H	1248					SV Unit code
4E1H	1249					TV Unit code
4E2H	1250					FV Unit code
4E3H	1251	System area	—	—	—	
4E4H	1252					
4E5H	1253					
4E6H	1254					
4E7H	1255					

**Tab. 3-22:** Buffer memory assignment of the ME1DA6HAI-Q (10/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled



Address		Description	Default	R/W*	Reference	
Hexa-decimal	Decimal					
4E8 <sub>H</sub>	1256	CH6 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27	
to	to					Tag
4EB <sub>H</sub>	1259					Message
4EC <sub>H</sub>	1260					
to	to					Descriptor
4FB <sub>H</sub>	1275					
4FC <sub>H</sub>	1276					
to	to					Manufacturer ID / Expanded manufacturer ID (HART 7)
503 <sub>H</sub>	1283					
504 <sub>H</sub>	1284					Device Type / Expanded device type (HART 7)
505 <sub>H</sub>	1285					
506 <sub>H</sub>	1286					Device ID
507 <sub>H</sub>	1287					
508 <sub>H</sub>	1288					Revisions
509 <sub>H</sub>	1289					
50A <sub>H</sub>	1290					Device function flags
50B <sub>H</sub>	1291					
to	to	Long tag				
51A <sub>H</sub>	1306					
51B <sub>H</sub>	1307	Private label distributor code (HART 7)				
51C <sub>H</sub>	1308					
51D <sub>H</sub>	1309	System area	—	—	—	
51E <sub>H</sub>	1310	CH6 Information about HART device	0000 <sub>H</sub>	R	Section 3.5.27	
51F <sub>H</sub>	1311					Final assembly number
520 <sub>H</sub>	1312					Date
521 <sub>H</sub>	1313					
522 <sub>H</sub>	1314					Write Protect
523 <sub>H</sub>	1315					PV range unit code
524 <sub>H</sub>	1316					PV Upper range value
525 <sub>H</sub>	1317					
526 <sub>H</sub>	1318					PV Lower range value
527 <sub>H</sub>	1319					
528 <sub>H</sub>	1320					PV Damping value
529 <sub>H</sub>	1321					
52A <sub>H</sub>	1322					Transfer function
52B <sub>H</sub>	1323	PV Unit code				
52C <sub>H</sub>	1324	SV Unit code				
52D <sub>H</sub>	1325	TV Unit code				
52E <sub>H</sub>	1326	FV Unit code				
52F <sub>H</sub>	1327	System area	—	—	—	

**Tab. 3-23:** Buffer memory assignment of the ME1DA6HAI-Q (11/11)

\* Indicates whether reading from and writing to a sequence program are enabled.  
R : Read enabled  
W : Write enabled

### 3.5.2 CH□ digital value (Un\G1 to Un\G6)

- This area is used by the programmable controller CPU to write digital values for performing D/A conversion. These values are written as 16-bit signed binary code.
- If a value outside the settable range is written, the upper or lower limit value of the range is used for D/A conversion. Also, if this happens, a check code and an error code will be stored in the Set value check code (Un\G11 to Un\G16) and Error code (Un\G19) respectively.

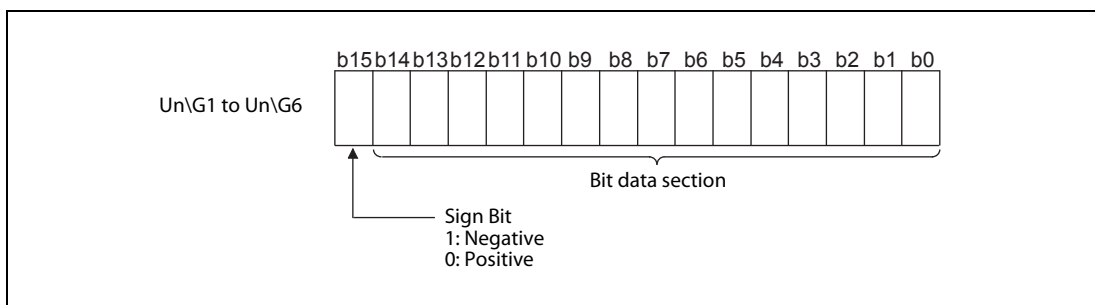


Fig. 3-12: The digital values are stored in 16-bit signed binary format

Output range setting	Digital input value	
	Normal range	Tight shut off
4 to 20 mA	-7000 to 28000	31500
0 to 20 mA	0 to 28000	30800

Tab. 3-24: Output range setting and digital value range

Digital input values below 0 in the 4 to 20 mA setting range result in output currents smaller than 4 mA. Negative output currents are not allowed. The output characteristics are shown in the following figure.

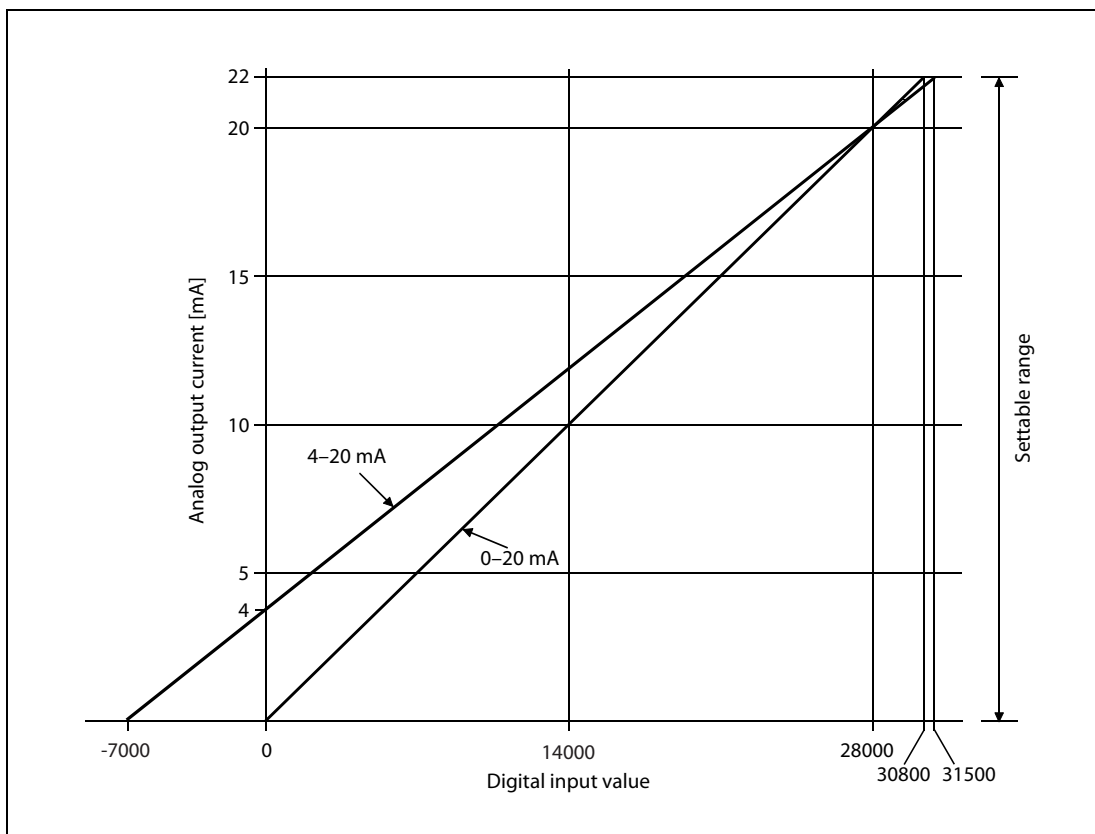


Fig. 3-13: Output characteristics of the ME1DA6HAI-Q

### 3.5.3 CH□ set value check codes (Un\G11 to Un\G16)

- Digital values set in CH□ Digital value (Un\G1 to Un\G6) are checked and if any of them is outside the settable range, the check result is stored in this area.
- When a digital value outside the settable range is written, one of the check codes listed in the table below is stored.

Check code	Description
000FH	A digital value exceeding the valid range was written.
00F0H	A digital value that falls short of the valid range was written.
00FFH	A digital value that either falls short or exceeds the valid range was written. For example, the 00FFH check code is stored if a digital value exceeding the valid range was written, and then, without the check code being reset, a digital value that falls short of the valid range was written.

**Tab. 3-25:** Set value check codes

- Once a check code is stored, it will not be reset even if the digital value is within the valid range.
- To reset the CH□ set value check code, set the error clear request (YF) to ON after rewriting the digital value so that it is within the valid range.

### 3.5.4 Error code (Un\G19)

- An error code generated by the D/A converter module is stored in the buffer memory address Un\G19.
- For more details of the error codes, please refer to section 6.1.

### 3.5.5 Setting range (Un\G20, Un\G21)

These read only areas can be used to confirm the setting ranges of the respective channels. For the setting use the intelligent function module switches in the PLC parameters (refer to section 4.5.2).

	b15	to	b12	b11	to	b8	b7	to	b4	b3	to	b0
Un\G20	CH4			CH3			CH2			CH1		
Un\G21	— (0H)			— (0H)			CH6			CH5		

**Fig. 3-14:** The setting range information of all channels is stored in two buffer memory addresses.

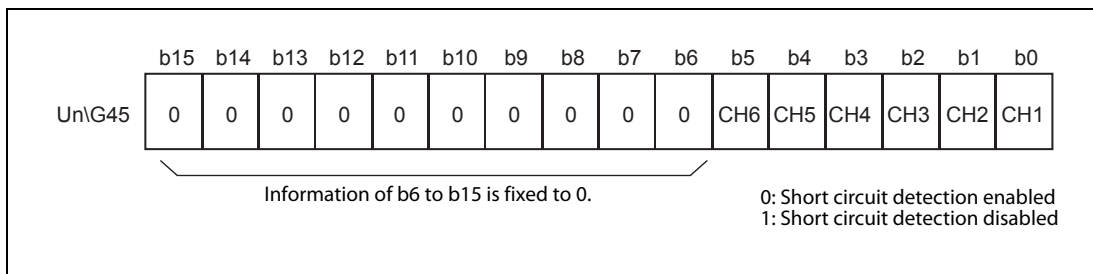
The correlation between the output range and the settings in Un\G20 and Un\G21 is shown in the following table.

Output range	Setting value
4 to 20 (mA)	0H
0 to 20 (mA)	1H
Illegal (not allowed)	Other settings

**Tab. 3-26:** Output ranges of the ME1DA6HAI-Q

### 3.5.6 Short circuit detection setting (Un\G45)

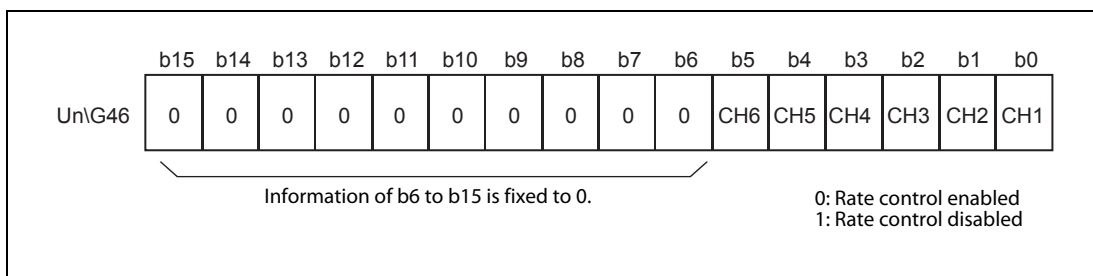
- This area is used to define whether to enable or disable the short circuit detection on each channel. (Refer to section 3.3.7.)
- To validate the short circuit detection setting, the operating condition setting request (Y9) must be turned ON/OFF. (Refer to section 3.4.2.)
- All channels are set to disable as the default setting.



**Fig. 3-15:** Assignment of the bits in buffer memory address 45

### 3.5.7 Rate control enable/disable setting (Un\G46)

- This area is used to define whether to enable or disable the rate control on each channel. (Refer to section 3.3.3.)
- To validate the rate control setting, the operating condition setting request (Y9) must be turned ON/OFF. (Refer to section 3.4.2)
- All channels are set to disable as the default setting.



**Fig. 3-16:** Assignment of the bits in buffer memory address 46

### 3.5.8 Disconnection detection/warning output setting (Un\G47)

- This area is used to set whether to enable or disable the disconnection detection and warning output on each channel. (For the disconnection detection, refer to section 3.3.6, and for the warning output refer to section 3.3.5.)
- To validate the disconnection detection/warning output setting, the operating condition setting request (Y9) must be turned ON/OFF. (Refer to section 3.4.2)
- As default, the disconnection detection and the warning output is disabled for all channels.

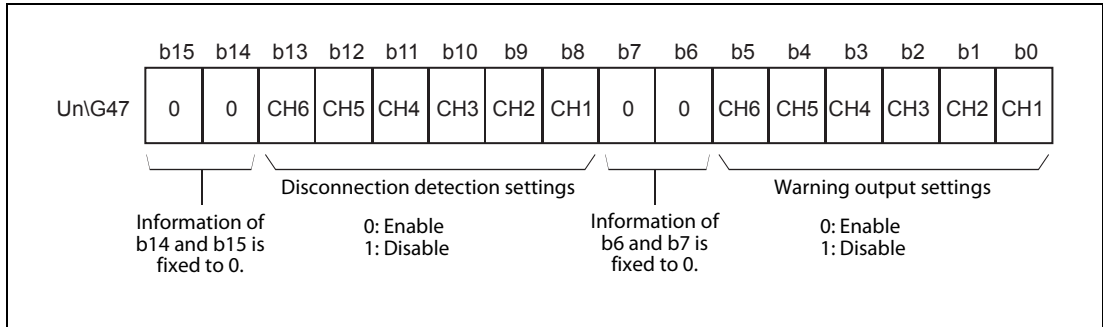


Fig. 3-17: Assignment of the bits in buffer memory address 47

### 3.5.9 Warning output flags (Un\G48)

- When the digital input value falls outside the CH□ warning output upper limit value/lower limit value (buffer memory addresses Un\G86 to Un\G97) range, the bit corresponding to the channel turns to "1". (Refer to section 3.3.5)
- Whether the warning is the upper or lower limit value warning can be checked on each channel.
- If a warning is detected on any of the channels enabled for conversion, the warning output signal (XE) also turns ON.
- Turning ON the operating condition setting request (Y9) or warning output clear request (YE) clears the warning output flag.

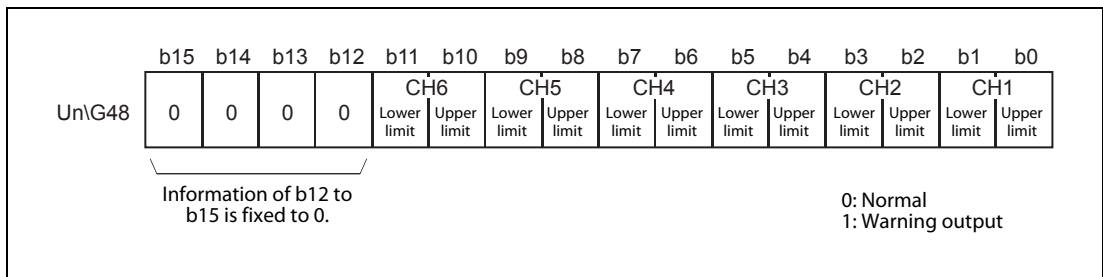
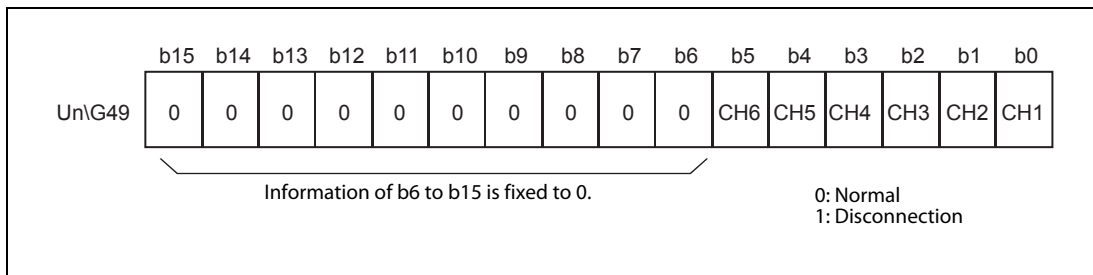


Fig. 3-18: Assignment of the bits in buffer memory address 48

### 3.5.10 Disconnection detection flags (Un\G49)

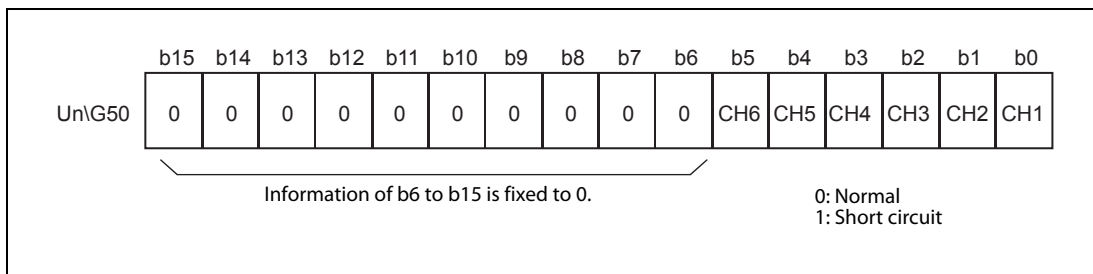
- If a disconnection occurs while an output of 4 mA or more is set, the bit corresponding to the channel turns to "1". (Refer to section 3.3.6)
- In addition, the disconnection detection signal (XD) also turns ON if a disconnection is detected on any channel.
- When the operating condition setting request (Y9) or disconnection detection clear request (YD) is turned ON, the disconnection detection flags are cleared.



**Fig. 3-19:** Assignment of the bits in buffer memory address 49

### 3.5.11 Short circuit detection flag (Un\G50)

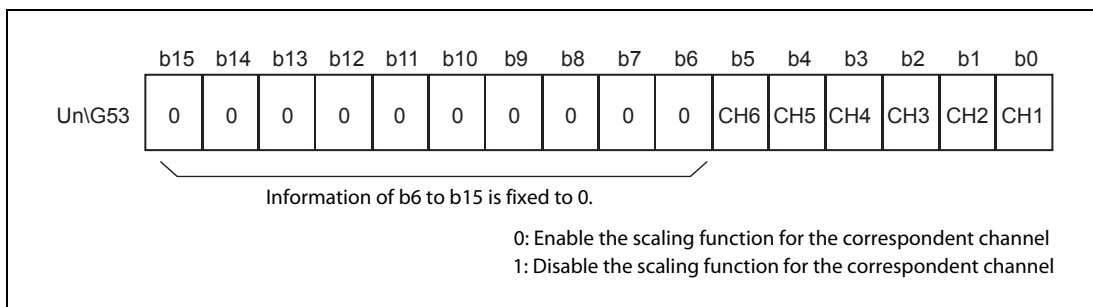
- In case of a short circuit, the bit corresponding to the channel turns to "1".
- If a short circuit is detected on any channel, the short circuit detection signal (X10) also turns ON.
- The short circuit detection flags are cleared when the operating condition setting request (Y9) or short circuit clear request (Y10) is turned ON.



**Fig. 3-20:** Assignment of the bits in buffer memory address 50

### 3.5.12 Scaling enable/disable setting (Un\G53)

- Whether to enable or disable the scaling function for each channel is set in this area.
- To validate the scaling function, the operating condition setting request (Y9) must be turned ON/OFF. (Refer to section 3.4.2)
- The default setting for all channels is "Disable".



**Fig. 3-21:** Assignment of the bits in buffer memory address 53

### 3.5.13 CH□ scaling upper/lower limit values (Un\G54 to Un\G65)

- Set a scaling conversion range for each channel.
- To validate the settings, the operating condition setting request (Y9) must be turned ON/OFF. (Refer to section 3.4.2)
- The setting range is -32768 to 32767.

For details of the scaling function, refer to section 3.3.4.

**NOTES**

Setting a value outside the above setting range or a value that does not meet the inequality "Upper limit > Lower limit" will cause an error. If this occurs, an error code is stored in the buffer memory address Un\G19, the Error flag (XF) is switched ON, and the module will operate under the setting before the error.

Since the default setting is 0, changing of the setting is required for operation.

When the Scaling enable/disable setting (Un\G53) is set to "Disable", scaling upper/lower limit values are ignored.

### 3.5.14 CH□ Increase/decrease digital limit values (Un\G70 to Un\G81)

- For rate control, set the range where the digital value can be incremented and decremented in a single conversion cycle (10 ms). (Refer to section 3.3.3.)
- The setting range is 0 to 32000. If any value outside the setting range is set, an error occurs and the corresponding error code is stored in buffer memory address Un\G19.
- The operating condition setting request (Y9) must be turned ON/OFF to validate the increase digital limit values and decrease digital limit values. (Refer to section 3.4.2.)

### 3.5.15 CH□ Warning output upper/lower limit values (Un\G86 to Un\G97)

- Set the upper and lower limit values of the digital input value for providing the warning output. (Refer to section 3.3.5.)
- The setting range is -32768 to 32767. Make the settings so that the upper limit value is greater than the lower limit value. If any value outside the setting range is set, an error occurs and the corresponding error code is stored in buffer memory address Un\G19.
- To validate the settings, the operating condition setting request (Y9) must be turned ON/OFF (Refer to section 3.4.2.)

### 3.5.16 HART enable (Un\G160)

- After the bit corresponded to each channel is set, HART communication will be automatically started in the indicated channel.

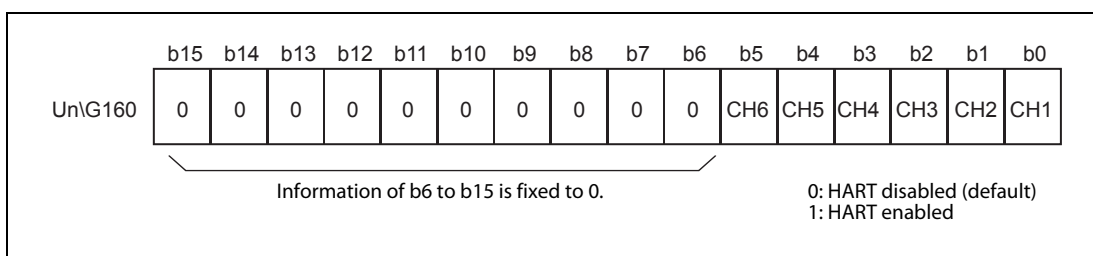


Fig. 3-22: Assignment of the bits in buffer memory address 160

**NOTE**

HART communication will be stopped without notification for output currents lesser than 2 mA. Depending on the specifications of the connected HART slave, communication may stop earlier at currents lesser than 4 mA (refer to the slave specification for the minimum current). It will recover automatically if the output current is 2 mA or higher again. The HART scan list (Un\G161, section 3.5.17) can be used to check the status of each HART device.

### 3.5.17 HART scan list (Un\G161)

- After HART functionality is enabled, the ME1DA6HAI-Q will automatically detect the HART device which is connected with the enabled channel. After the device information are stored into the buffer memory, the corresponding bit in the "HART Scan list" is set. (Refer to the figures below.)

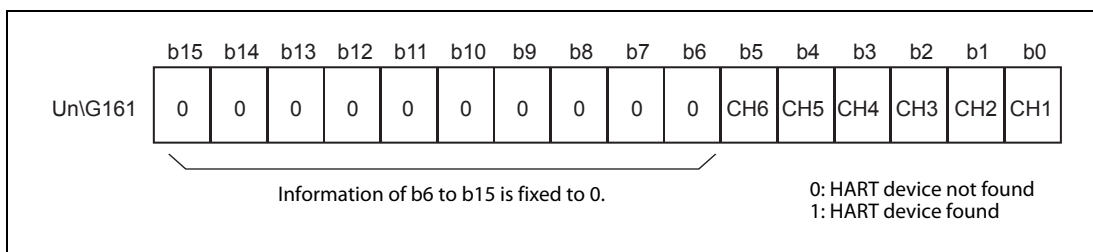
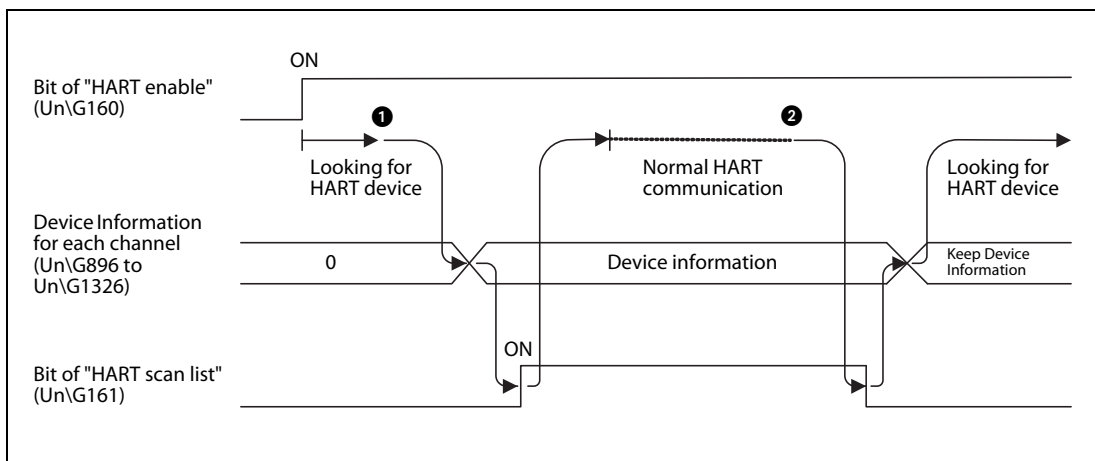


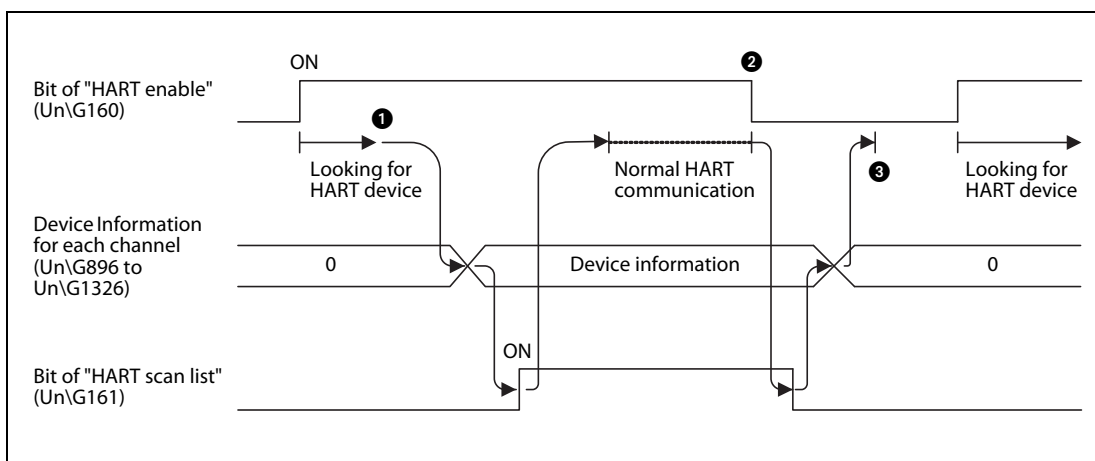
Fig. 3-23: Assignment of the bits in the HART scan list (buffer memory address 161)





**Fig. 3-24:** Operation when HART device is detected and missing

- ❶ When a HART device is detected, the device information is stored, the HART communication is initialized, and the corresponding bit in the HART scan list is set.
- ❷ When the HART communication is interrupted due to a missing HART device, the corresponding bit in the HART scan list is reset and the HART device information is kept.



**Fig. 3-25:** Operation when HART functionality is disabled

- ❶ When a HART device is detected, the device information is stored, the HART communication is initialized, and the corresponding bit in the HART scan list is set.
- ❷ When the HART communication is disabled, the corresponding bit in the HART scan list is reset and the HART device information is cleared.
- ❸ Since the HART enable bit in Un\G160 is reset, the HART communication is stopped.

### 3.5.18 HART cycle time (Un\G162 to Un\G164)

- The current, maximum and minimum HART cycle time is stored in Un\G162, Un\G163 and Un\G164 respectively.
- The HART cycle time is the total time required for accessing each HART enabled channel or rather the time period between two accesses to the same HART channel.
- The unit of the HART cycle time is 10 ms.
- These values are reset after a power reset or PLC CPU reset.

### 3.5.19 HART maximum retries (Un\G176 to Un\G181)

- Set the maximum number of command retries for each HART channel.
- The range is 0 to 30, default is 3 retries.

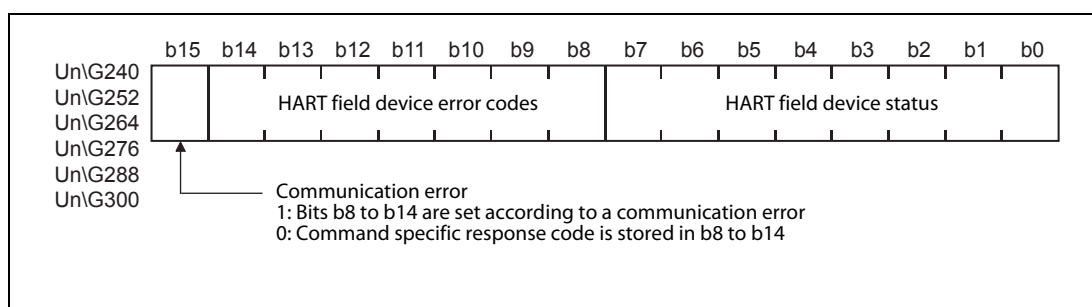
### 3.5.20 HART device information refresh interval (Un\G191)

- Set the maximum interval in which the device information shall be read from a HART device.
- The range is 0 to 60 seconds, default is 30 seconds.
- This setting can speed up the FDT/DTM communication when changing configuration data via the DTM.

The affected HART device information data is located in the buffer memory addresses Un\G896 to Un\G1326. The HART Process Variables (Un\G240 to Un\G311) are not affected, they are updated cyclically.

### 3.5.21 HART field device status (Un\G240, Un\G252, Un\G264...)

Information about the status of the HART field device are stored in the corresponding buffer memory address (Channel 1: Un\G240, CH 2: Un\252, CH 3: Un\G264 etc.).



**Fig. 3-26:** Assignment of bits for HART field device error codes and status

The meaning of the bits b0 to b7 is as follows:

Bit	Meaning (when bit is set to "1")
b0	Primary variable out of limits
b1	Non-primary variable out of limits
b2	Loop current saturated
b3	Loop current fixed
b4	More status available
b5	Cold start
b6	Configuration changed
b7	Device malfunction

**Tab. 3-27:** HART field device status

Whether the bits b8 to b14 store information about a communication error or a command specific response code is indicated by b15:

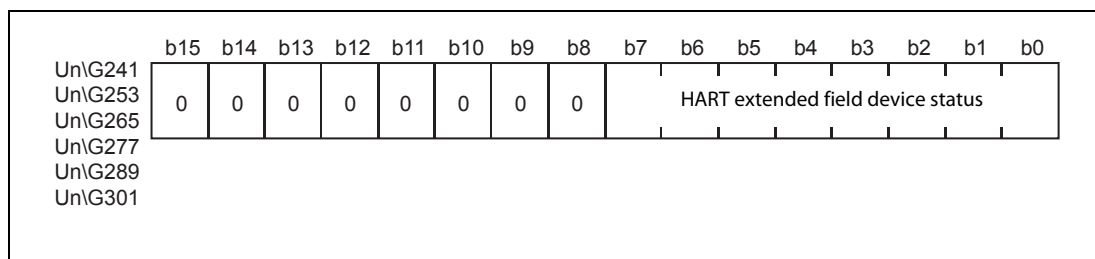
Bit	When b15 is "1": Communication error	When b15 is "0": Command specific response code*
	Meaning (when bit is set to "1")	The code is the binary value of the bits b8 to b14.
b8	—	0: No error 5: Not enough data received 6: Device command error 7: Write protection 16: Access restricted 32: Device busy 64: Command not implemented
b9	Buffer overrun	
b10	—	
b11	Checksum error	
b12	Framing error	
b13	UART overrun	
b14	Parity error	

**Tab. 3-28:** HART field device error codes

\* Listed in this table are some commonly used codes. For the codes available for the connected HART field device, please refer to the instruction manual of the device.

### 3.5.22 Extended HART field device status (Un\G241, Un\G253, Un\G265...)

Information about the extended status of the HART field device are stored in the corresponding buffer memory address. (Channel 1: Un\G241, CH 2: Un\253, CH 3: Un\G265 etc.)



**Fig. 3-27:** Assignment of bits for HART extended field device status

The meaning of the bits b0 to b7 is as follows:

Bit	Meaning (when bit is set to "1")	Description
b0	Maintenance required	This bit is set to indicate that, while the device has not malfunctioned, the field device requires maintenance.
b1	Device variable alert	This bit is set if any device variable is in an alarm or warning state. The host should identify the device variable(s) causing this to be set using the device variable status indicators.
b2	Critical Power Failure	For devices that can operate from stored power. This bit is set when that power is becoming critically low. For example, a device powered by a rechargeable battery will set this bit if the battery voltage is becoming low. Devices must be able to sustain their network connection for at least 15 minutes from the moment when this bit is set. A device may disconnect from the network if its power level drops too low.
b3	—	—
b4	—	—
b5	—	—
b6	—	—
b7	—	—

**Tab. 3-29:** HART extended field device status

### 3.5.23 Device variable status (Un\G242 & Un\G243, Un\G254 & Un\G255...)

- The status of each HART device (process) variable according to the HART Command summary specification is stored in these buffer memory addresses.
- For each channel two buffer memory addresses are occupied.
- The Device Variable Status is read by HART command #9. If command #9 is not supported by the device, HART command #3 can be used instead. In this case the Device Variable Status is derived from the communication status ("Good" and "Bad" only).
- If a certain variable is not present in the device, the status is set to "bad".

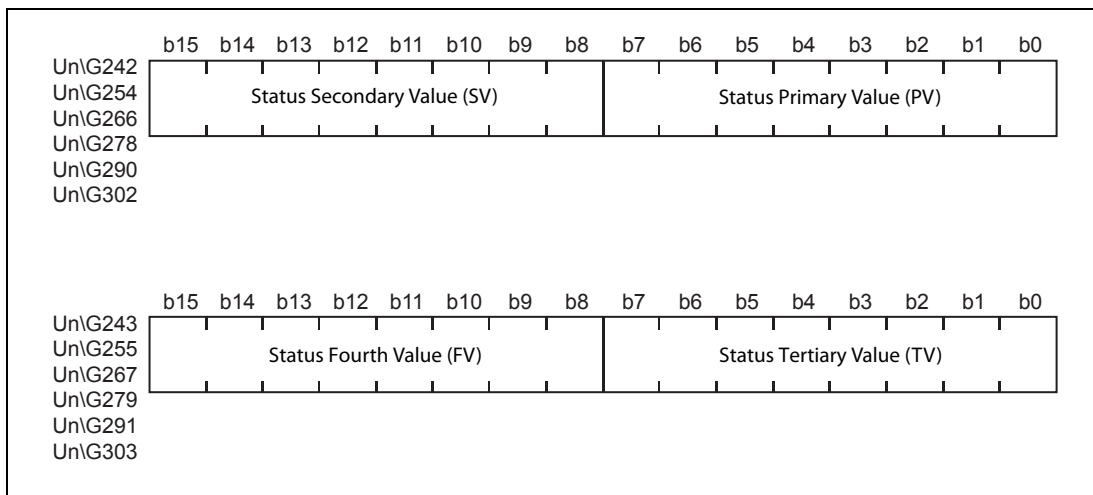


Fig. 3-28: The status of up to four device variables is stored

- Each status has the following structure.

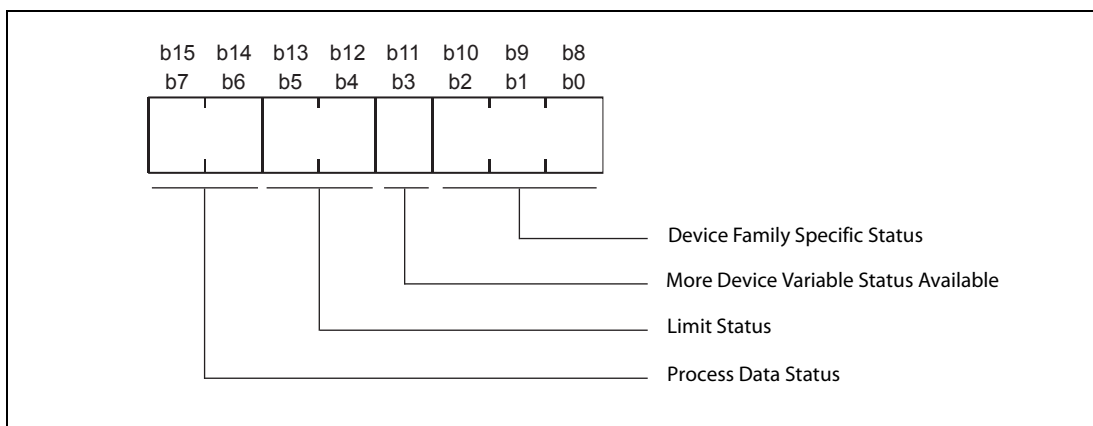


Fig. 3-29: Status structure

Item	Description	Remark
Device Family Specific Status	Device Family depended	—
More Device Variable Status Available	The availability of additional Device Family-specific status is stored. • 1 = More Device Variable Status available • 0 = More Device Variable Status not available	This bit indicates if the Device Family Specific Status is available via the Device Family Command.

Tab. 3-30: Contents of the Device Variable status

Item	Description	Remark
Limit Status	Shows whether the Device Variable value is limited. <ul style="list-style-type: none"> <li>• 11 = Constant</li> <li>• 01 = Low Limited</li> <li>• 10 = High Limited</li> <li>• 00 = Not Limited</li> </ul>	The combinations of these 4 bits within each status show the status of Device Variable's value. For example, if the Process Data Status is "Manual/Fixed" and the Limit Status is "Not Limited" then the value is being manually controlled.
Process Data Status	The overall status of the Device or Dynamic Variable value is stored. <ul style="list-style-type: none"> <li>• 11 = Good</li> <li>• 01 = Poor Accuracy</li> <li>• 10 = Manual/Fixed</li> <li>• 00 = Bad</li> </ul>	

**Tab. 3-30:** Contents of the Device Variable status

### 3.5.24 HART process variables (Un\G244 to Un\G251, Un\G256 to Un\G263...)

- These areas store the HART Process Variables as transmitted with command #9 or if not available with command #3.
- Up to four Process Variables are stored per channel.
- Each Process Variable occupies two successive buffer memory addresses. The values are stored as 32-bit floating point numbers.
- If a certain variable is not present the corresponding buffer memory addresses are set to NaN (not a number) which is 7FA0000H.

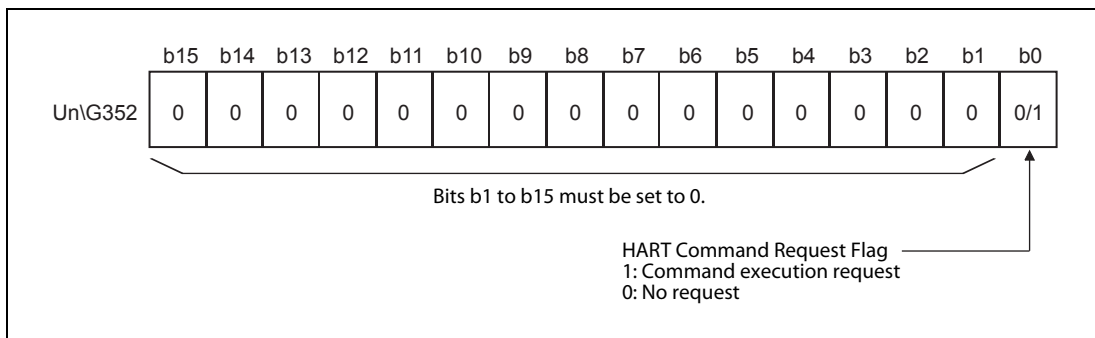
#### NOTE

For a detailed description of floating point numbers please refer to the Programming Manual for the A/Q series and the MELSEC System Q, art. no. 87431.

### 3.5.25 HART Command Request (Un\G352 to Un\G483)

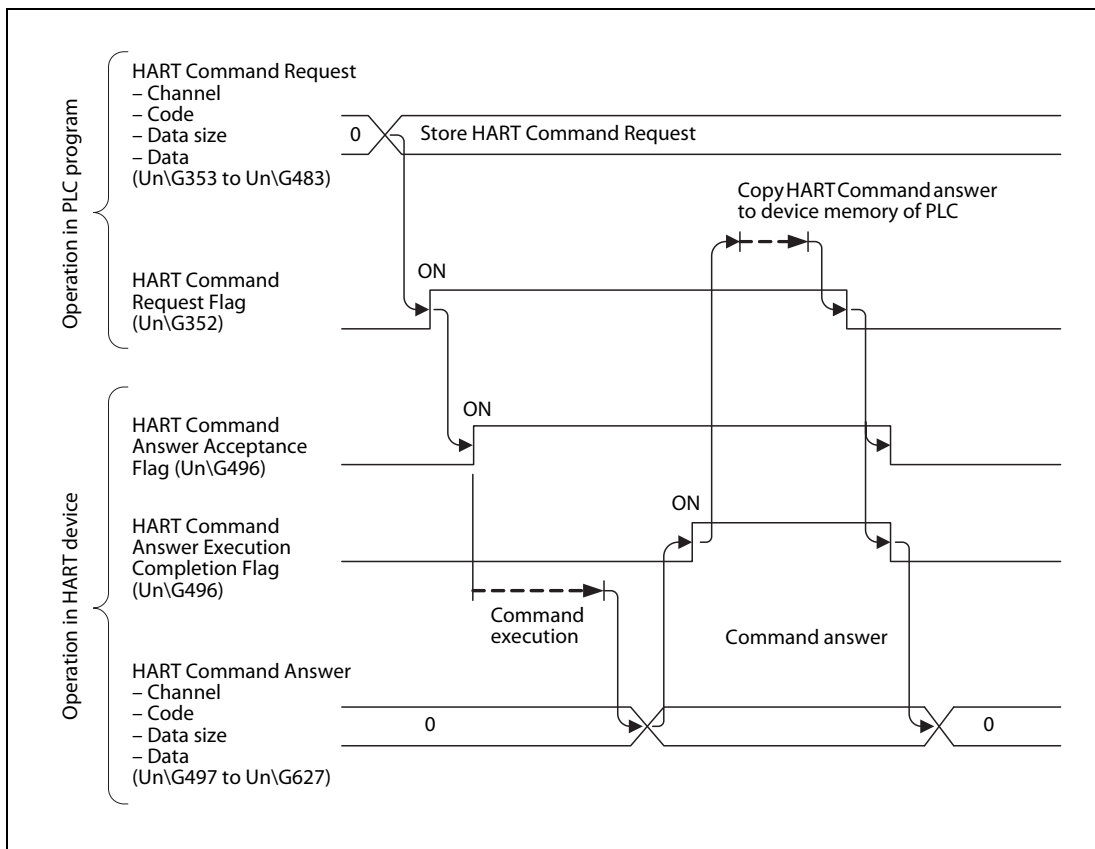
#### HART Command Request Flag (Un\G352)

- For execution of a HART command, set the HART Command Request Flag to "1".
- Set the HART Command, the contents of the data buffer and data size before setting this flag.
- When the HART Command Answer Flag is "1" the HART Command Request Flag shall be reset.



**Fig. 3-30:** Bit 0 of the buffer memory address Un\G352 is the request flag for a HART Command

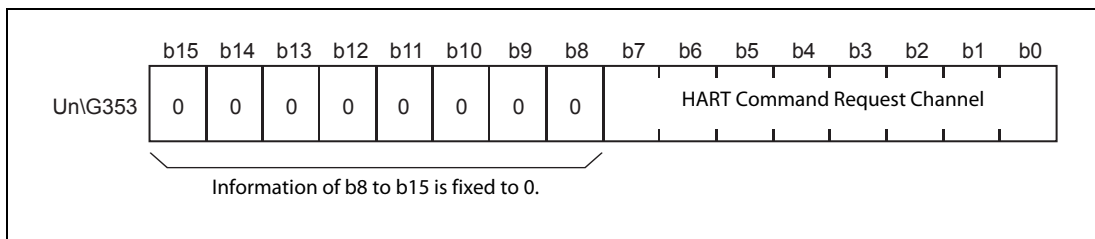
The operation for a HART Command Request and the appropriate answer is shown in the following figure.



**Fig. 3-31:** HART command execution chart

**HART Command Request Channel (Un\G353)**

- Un\G353 contains the channel number (1 to 6) to which the subsequent HART Command shall be sent.



**Fig. 3-32:** The contents of the high byte of Un\G353 is fixed to "0"

- The relation between the setting value for the HART Command Request Channel and the channel No. is as follows:

Setting value	Command Request Target Channel
1	Channel 1
2	Channel 2
3	Channel 3
4	Channel 4
5	Channel 5
6	Channel 6

**Tab. 3-31:** Channel selection

**HART Command Request Code (Un\G354)**

- Stores the HART command according to HART specification or the instruction manual of the HART transmitter.

**HART Command Request Data Size (Un\G355)**

- Stores the amount of valid data to be sent in the HART Data Buffer (Un\G356 to Un\G483).
- The maximum setting value is 255.

**HART Command Request Data (Un\G356 to Un\G483)**

- Data to be sent to a HART device is stored in these 128 buffer memory addresses.
- The amount of data is determined by the Data Size (Un\G355). Surplus data is ignored.

### 3.5.26 HART Command Answer (Un\G496 to Un\G627)

#### HART Command Answer Flag (Un\G496)

- The high byte (b8 to b15) of Un\G496 forms the HART Command Acceptance Flag. As a reaction of a HART Command Request (refer to section 3.5.25), the HART device writes one of the following two values into this byte:

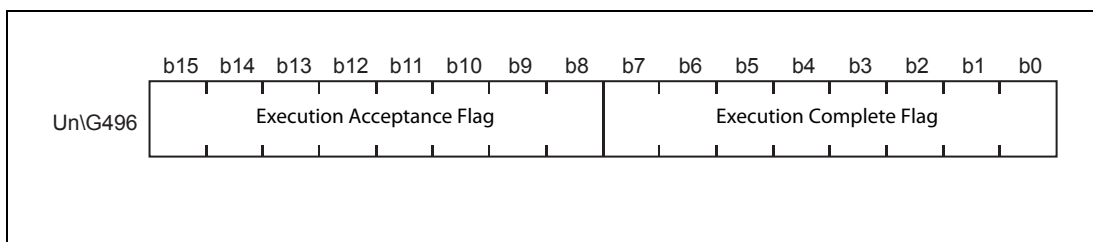
"0": Command not accepted or no request

"1": Command accepted

- The low byte (b0 to b7) contains the HART Command Execution Complete Flag. This byte has also only two states and is written by the HART device:

"0": Command not complete or no request

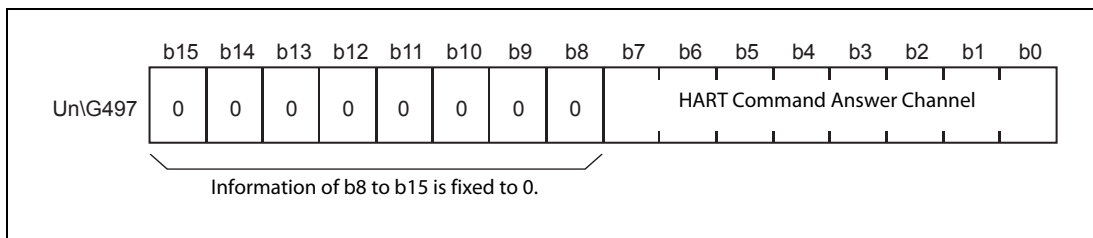
"1": Command complete.



**Fig. 3-33:** Un\G496 is shared by the Execution Acceptance Flag and the Execution Complete Flag

#### HART Command Answer Channel (Un\G497)

- The channel number which has received the subsequent HART Command Answer is stored in the low byte of Un\G497.
- Range for the channel number: 1 to 6



**Fig. 3-34:** The low byte of Un\G497 indicates the channel No.

#### HART Command Answer Code (Un\G498)

- Stores the HART command from the device's answer

#### HART Command Answer Data Size (Un\G499)

- Stores the amount of valid data in the HART Command Answer Data Buffer (Un\G500 to Un\G627).

#### HART Command Answer Data (Un\G500 to Un\G627)

- The received data from the device according to HART specification is stored in these 128 buffer memory addresses.
- The first two bytes are the device's status.



### 3.5.27 Information about HART Device (Un\G896 to Un\G966, Un\G968 to Un\G1038...)

Detailed information about the connected HART devices is stored in the following areas of the buffer memory:

HART device connected to channel	Information storage area
1	Un\896 to Un\966
2	Un\968 to Un\1038
3	Un\1040 to Un\1110
4	Un\1112 to Un\1182
5	Un\1184 to Un\1254
6	Un\1256 to Un\1326

**Tab. 3-32:** Assignment of buffer memory areas

The refresh interval for the HART device information can be set in buffer memory address Un\G191 (refer to section 3.5.20).

#### HART Tag

- The user defined HART Tag is read by HART Command #13.
- The Tag occupies four successive buffer memory addresses.
- 8 characters in ASCII format are stored, the first character in the low byte (LSB) of the lowest address.
- End of string is filled with space characters (20H).

#### HART Message

- The HART Message is read by HART Command #12.
- The Message occupies 16 successive buffer memory addresses.
- 32 characters in ASCII format are stored, beginning with the first character in the low byte (LSB) of the lowest address.
- End of string is filled with space characters (20H).

#### HART Descriptor

- The user defined HART Descriptor is read by HART Command #13.
- The Descriptor occupies 8 successive buffer memory addresses.
- 16 characters in ASCII format are stored, starting with the first character in the low byte (LSB) of the lowest address.
- End of string is filled with space characters (20H).

#### HART Manufacturer ID

- This indicates the manufacturer of the HART device. The name is given as a code established by the HART Communication Foundation and set by manufacturer.
- The Manufacturer ID is read by HART Command #0
- The amount of data depends on the HART Field Communications Protocol used:
  - HART 5/6: 1 byte
  - HART 7: 2 bytes

**Hart Device Type**

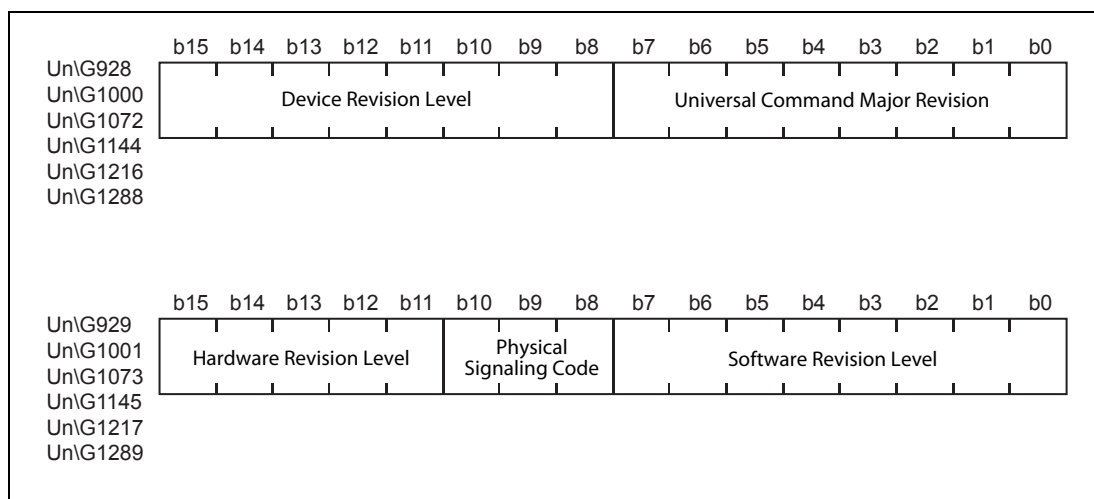
- The Hart Device Type is set by the manufacturer and read by HART Command #0.
- The amount of data depends on the HART Field Communications Protocol used:
  - HART 5/6: 1 byte
  - HART 7: 2 bytes

**HART Device ID**

- The HART Device ID is read by HART Command #0.
- Two successive buffer memory addresses are reserved for the Device ID.
- The Device ID occupies 3 bytes.

**HART Revisions**

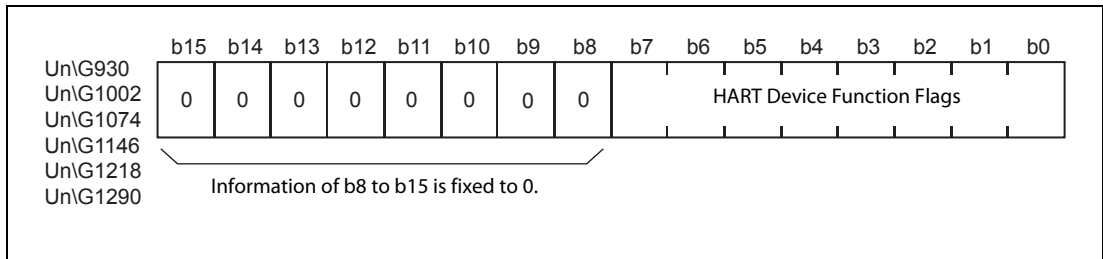
- The HART Revisions are set by the manufacturer and read by HART Command #0.
- The revision information occupies two successive buffer memory addresses.



**Fig. 3-35:** Various revision information is stored

**HART Device Function Flags**

- The HART Device Function Flags are read by HART Command #0.



**Fig. 3-36:** The flags are stored in the low byte of the corresponding buffer memory address.

The meaning of the bits b0 to b7 is as follows:

Bit	Meaning (when bit is set to "1")
b0	Multi-Sensor Field Device
b1	EEPROM Control
b2	Protocol Bridge Device
b3	IEEE 802.15.4 2.4GHz DSSS with O-QPSK Modulation
b4	—
b5	—
b6	C8psk Capable Field Device
b7	C8psk In Multi-Drop only

**Tab. 3-33:** HART Device Function Flags

**HART Long Tag**

- The Long Tag with international (ISO Latin 1) characters allows consistent implementation of the longer tag names required by many industry users.
- The HART Long Tag is read by HART Command #20.
- The Long Tag occupies 16 successive buffer memory addresses.
- 32 characters in ASCII format are stored, beginning with the first character in the low byte (LSB) of the lowest address.
- End of string is filled with space characters (20H).

**HART Private Label Distributor**

- This function is available with HART 7 only.
- The HART Private Label Distributor is read by HART Command #0 and consists of 2 bytes.

**HART Device Profile**

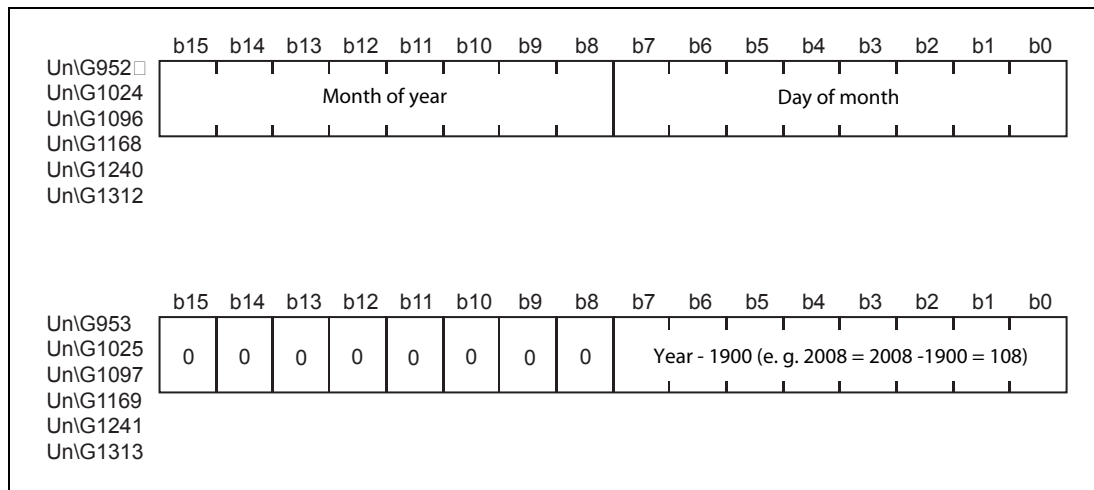
- This function is available with HART 7 only.
- The HART Device Profile is read by HART Command #0.
- The information is stored in 1 byte and in accordance with the HART Common Tables Specification (Table 57).

**HART Final Assembly Number**

- The HART Final Assembly Number is read by HART Command #16.
- Two successive buffer memory addresses are reserved for the Final Assembly Number.
- The received information is stored in 3 bytes.

**HART Date**

- The HART Date (date of last calibration) is read by HART Command #13.
- The received data is stored in two successive buffer memory addresses.



**Fig. 3-37:** The HART Date consists of information about day, month and year

**HART Write Protect**

- The HART Write Protect status is read by HART Command #15.
- One of the following three values is stored:
  - 0: Not write protected
  - 1: Write protected
  - 251: Write protection is not supported by the device

**HART PV Range Unit Code**

- The HART PV Range Unit Code is read by HART Command #15.
- The code indicates the units used for the range settings for the primary variable (PV). The code values are defined in the HART specification.

**HART PV Upper and Lower Range Value**

- The upper and lower range limits for the Primary Variable (PV) are read by command #15.
- For each range value two successive buffer memory addresses are reserved. The values are stored as 32-bit floating point numbers.

**NOTE**

For a detailed description of floating point numbers please refer to the Programming Manual for the A/Q series and the MELSEC System Q, art. no. 87431.

**HART PV Damping Value**

- Damping constant for the primary variable (PV) in seconds, read by HART command #15.
- The Damping Value is stored in two successive buffer memory addresses as a 32-bit floating point number.

**NOTE**

For a detailed description of floating point numbers please refer to the Programming Manual for the A/Q series and the MELSEC System Q, art. no. 87431.

**HART Transfer Function**

- The HART Transfer Function is read by HART command #15.
- The code values are defined in the HART specification.

**HART Unit Code (PV, SV, TV and FV)**

- The HART Unit Code for the process variables is read by HART Commands #3 or #9.
- The code indicates the units used for the respective data item. The code values are defined in the HART specification.



## 4 Setup and Procedures before Operation

### 4.1 Handling Precautions

- Do not drop the module or subject it to heavy impact.
- Do not remove the PCB of the module from its case. Doing so may cause the module to fail.
- Prevent foreign matter such as dust or wire chips from entering the module. Such foreign matter can cause a fire, failure, or malfunction.
- Before handling the module, touch a grounded metal object to discharge the static electricity from the human body.

Failure to do so may cause the module to fail or malfunction.

- Tighten the screws such as module fixing screws within the following ranges. Loose screws may cause short circuits, failures, or malfunctions.

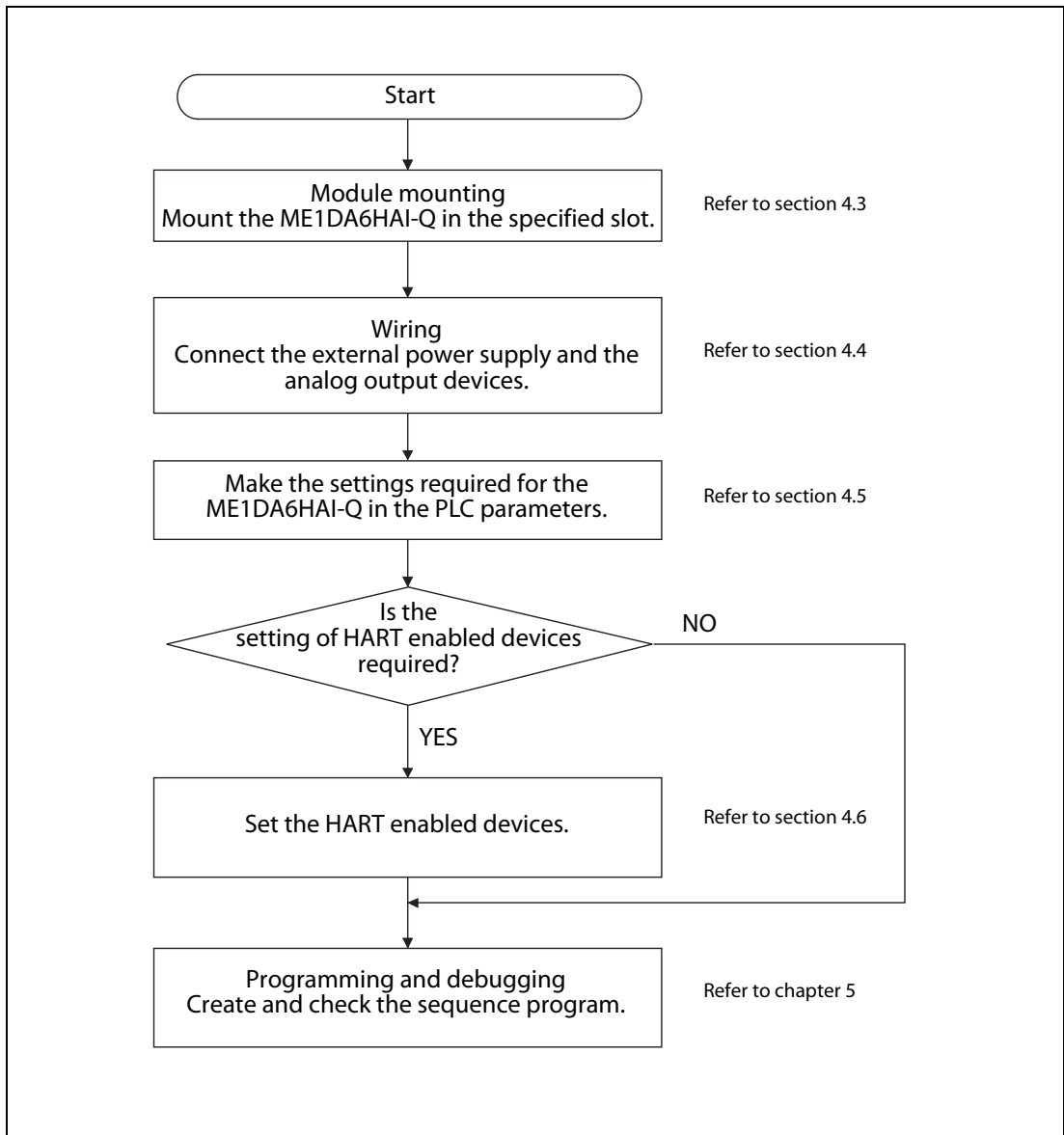
Screw location	Tightening torque range
Module fixing screw (M3 screw, optional)	0.36 to 0.48 Nm
Terminal block screws (M3 screws)	0.42 to 0.58 Nm
Terminal block mounting screws (M3.5 screws)	0.66 to 0.89 Nm

**Tab. 4-1:** Tightening torques

- To mount the module on the base unit, fully insert the module fixing latch into the fixing hole in the base unit and press the module using the hole as a fulcrum.

Improper installation may result in a module malfunction, or may cause the module to fall off.

## 4.2 Setup and Procedures before Operation



**Fig. 4-1:** Function chart for the setup of the HART analog output module



## 4.3 Installation of the Module

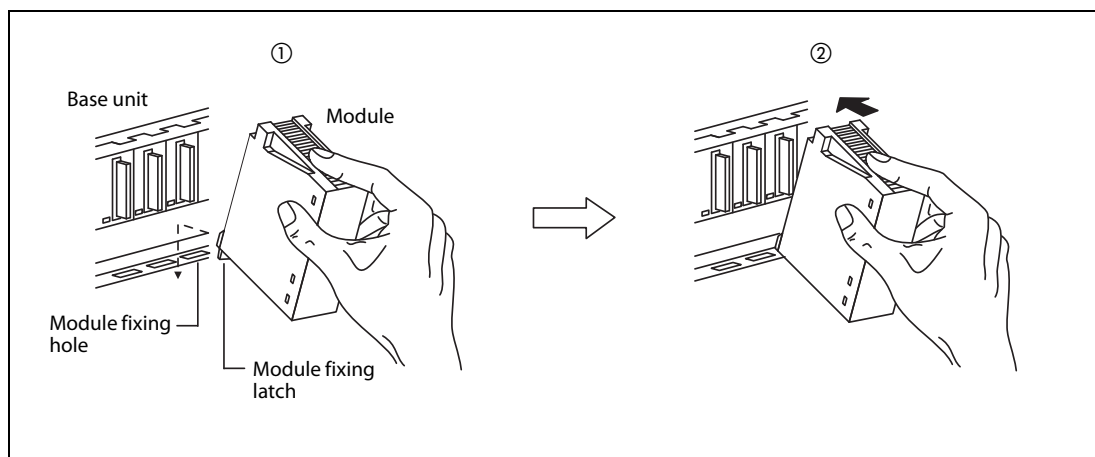
The ME1DA6HAI-Q can be combined with a CPU module or, when mounted to a remote I/O station, with a master module for MELSECNET/H (refer to section 2.1).



### CAUTION:

- **Cut off all phases of the power source externally before starting the installation or wiring work.**
- **Always insert the module fixing latch of the module into the module fixing hole of the base unit. Forcing the hook into the hole will damage the module connector and module.**
- **Do not touch the conductive parts of the module directly.**

- ① After switching of the power supply, insert the module fixing latch into the module fixing hole of the base unit.
- ② Push the module in the direction of the arrow to load it into the base unit.



**Fig. 4-2:** Module installation

- ③ Secure the module with an additional screw (M3 x 12) to the base unit if large vibration is expected. This screw is not supplied with the module.

## 4.4 Wiring

### 4.4.1 Wiring precautions

In order to optimize the functions of the HART analog output module and ensure system reliability, external wiring that is protected from noise is required. Please observe the following precautions for external wiring:

- Use separate cables for the AC control circuit and the external output signals of the analog output module to prevent influences of AC surge or induction.
- Do not lay cables for analog signals close to the main circuit, high-voltage power lines, or load lines. Otherwise effects of noise or surge induction are likely to take place. Keep a safe distance of more than 100 mm from the above when wiring.
- The FG terminal of ME1DA6HAI-Q must be connected to the ground certainly.
- The shield wire or the shield of the shielded cable must be grounded at one end.
- Observe the following items for wiring the terminal block. Ignorance of these items may cause electric shock, short circuit, disconnection, or damage of the product:
  - Use solderless terminals for the connection. Twist the end of stranded wires and make sure there are no loose wires.
  - Solderless terminals with insulating sleeves cannot be used for the terminal block. Covering the cable-connection portion of the solderless terminal with a marked tube or an insulation tube is recommended.
  - Do not solder-plate the electric wire ends.
  - Connect only electric wires of regular size.
  - Tightening of terminal block screws should follow the torque described on the previous page.
  - Fix the electric wires so that the terminal block and connected parts of electric wires are not directly stressed.
- When wiring to the module placed on the right side of the ME1DA6HAI-Q is difficult, remove the ME1DA6HAI-Q before wiring.

## 4.4.2 External wiring

The ME1DA6HAI-Q is designed for current output only. Devices requiring a current input for instance as setting value such as actuators, servo amplifiers or inverters can be connected. It is also possible to mix standard (not HART enabled) devices with HART devices. For HART enabled devices, no additional wiring is required since the analog output wiring is used for communication between the ME1DA6HAI-Q and the device (refer to section 3.3.8).

To each output channel of the ME1DA6HAI-Q one HART enabled device can be connected in a point-to-point configuration. Multidrop network connection (more than one device to one channel) is not possible.

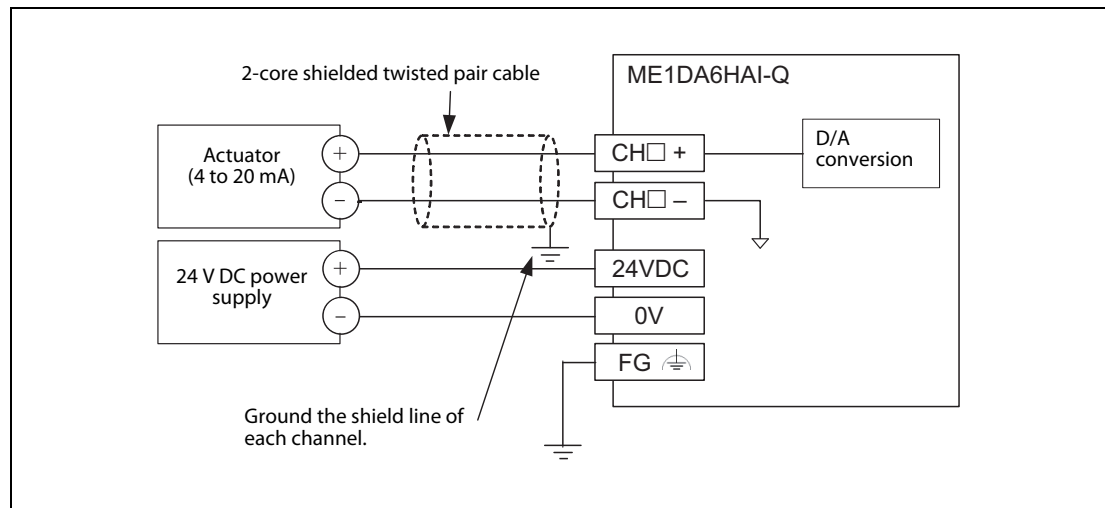
### Applicable cables

Concerning to the applicable cable, refer to the HART specification for more details.

### External power supply

For operation of the ME1DA6HAI-Q, an external power supply of 24 V DC (+20%, -15%, which gives a voltage range of 20.4 to 28.8 V DC), is required.

### Connection of the external wiring



**Fig. 4-3:** External wiring of the HART analog output module

## 4.5 PLC Parameter Setting

In the PLC parameters the I/O assignment for the ME1DA6HAI-Q, the analog output range for each channel and the HOLD/CLEAR function are set.

**NOTE**

For setting the parameters of the ME1DA6HAI-Q, the intelligent function utility of GX Works2 can be used also (please refer to chapter 5).

### 4.5.1 I/O assignment

Start GX Developer or GX IEC Developer and open up the project with the ME1DA6HAI-Q. After the selection of **Parameter** in the Project Navigator Window, double-click on **PLC parameter**. The Q parameter setting window will appear. Click on the **I/O assignment** tab.

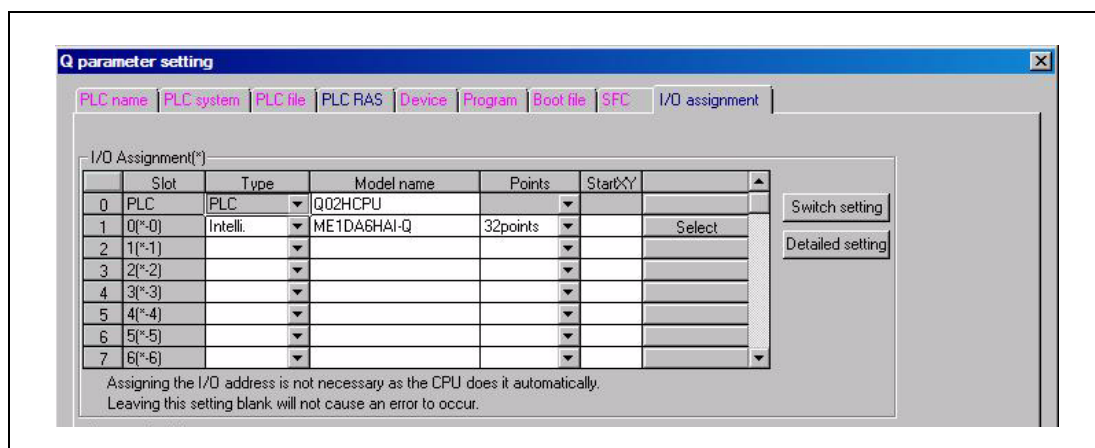


Fig. 4-4: I/O assignment setting screen

Set the following for the slot in which the ME1DA6HAI-Q is mounted:

- Type:** Select "Intelli."
- Model name:** ME1DA6HAI-Q (Entering of the module model name is optional. The entry is used for documentation only and has no effect on the function of the module.)
- Points:** Select 32 points.
- StartXY:** Start I/O number for the ME1DA6HAI-Q. (Assigning of the I/O address is not necessary as the address is automatically assigned by the PLC CPU.)

When using in the standard system configuration (on the main or extension base), select **Detailed settings** to specify the control CPU of the ME1DA6HAI-Q in a multiple CPU system. It is unnecessary to set the "Error time output mode" or "H/W error time PLC operation mode" since these settings are invalid for the ME1DA6HAI-Q.

When the ME1DA6HAI-Q is mounted to a MELSECNET/H remote I/O station, if the analog output is to be held in the case of a link error, "Error time output mode" (in the **Detailed settings**) must be set to "Hold". (Refer to section 3.3.1 for further details.)

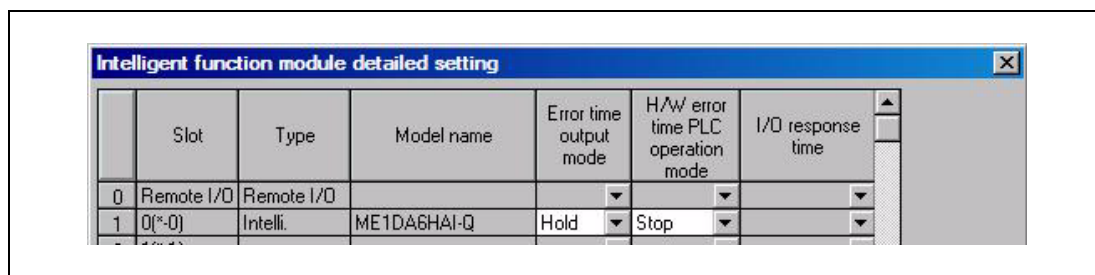
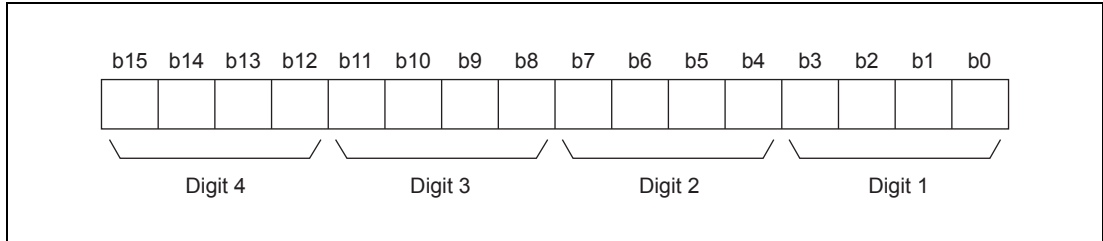


Fig. 4-5: Detailed settings for intelligent function modules

### 4.5.2 Intelligent function module switch settings

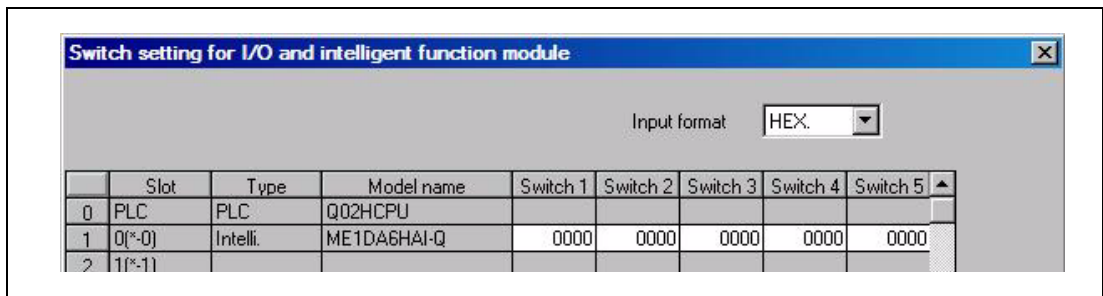
The analog output range for each channel of the ME1DA6HAI-Q is selected by two "switches" in the PLC parameters. There are no switches at the module itself.

The intelligent function module switches are set using 16 bit data (4 hexadecimal digits).



**Fig. 4-6:** Bit assignment for one switch

In the I/O assignment setting screen (section 4.5.1) click on **Switch setting** to display the screen shown below, then set the switches as required. The switches can easily be set if values are entered in hexadecimal. Change the entry format to hexadecimal and then enter the values.



**Fig. 4-7:** Switch setting for intelligent function module screen

When the intelligent function module switches are not set, the default value for switches 1 to 5 is 0000H.

Switch	Setting item							
Switch 1	Output range setting (CH1 to CH4) 	<table border="1"> <thead> <tr> <th>Analog output range</th> <th>Output range setting value</th> </tr> </thead> <tbody> <tr> <td>4 to 20 mA</td> <td>0H</td> </tr> <tr> <td>0 to 20 mA</td> <td>1H</td> </tr> </tbody> </table>	Analog output range	Output range setting value	4 to 20 mA	0H	0 to 20 mA	1H
Analog output range	Output range setting value							
4 to 20 mA	0H							
0 to 20 mA	1H							
Switch 2	Output range setting (CH5 and CH6) 	Output range setting values other than 0H or 1H are not allowed.						
Switch 3	HOLD/CLEAR function setting (CH1 to CH6) 	HOLD/CLEAR function setting 0: CLEAR 1: HOLD						
Switch 4	Reserved	Fixed to 0H						

**Tab. 4-2:** Switch settings for the ME1DA6HAI-Q

Switch	Setting item
Switch 5	<p>The HART specification limits the rise time of the analog signal to avoid communication problems. Due to this rise time limitation the conversion time with enabled HART communication is slower than without HART communication.</p> <p>This setting can be used to make the conversion time with HART communication as fast as the conversion time without HART communication.</p> <p>0: Fast conversion mode with HART communication disabled 1: Fast conversion mode with HART communication enabled</p> <p>The default setting of 0000H will ensure compliance with the HART communication standard.</p> <p><b>Caution:</b> When the fast conversion mode with HART communication is enabled, errors may occur in case of rapid changes of the output signal. Increase the retry values in the buffer memory addresses Un\G176 to Un\G181 to remedy these errors.</p>

Tab. 4-2: Switch settings for the ME1DA6HAI-Q

**NOTE**

When the ME1DA6HAI-Q is mounted to a MELSECNET/H remote I/O station, the HOLD/CLEAR setting by the intelligent function module switch is invalid. (Refer to section 3.3.1.)

● Setting example

The configuration shown below is used for the setting example.

Channel	Output range		HOLD/CLEAR function setting		Fast conversion mode with HART communication	
	0 to 20 mA	4 to 20 mA	HOLD	CLEAR	Disabled	Enabled
1		●		●		●
2	●		●		●	
3	●		●		●	
4		●		●	●	
5		●		●		●
6	Not connected		Not connected		Not connected	

Tab. 4-3: Output ranges and HOLD/CLEAR settings for this example

Setting value for switch 1: 0110H

Setting value for switch 2: 0000H

Setting value for switch 3: 0000 0000 0000 0110 = 0006H

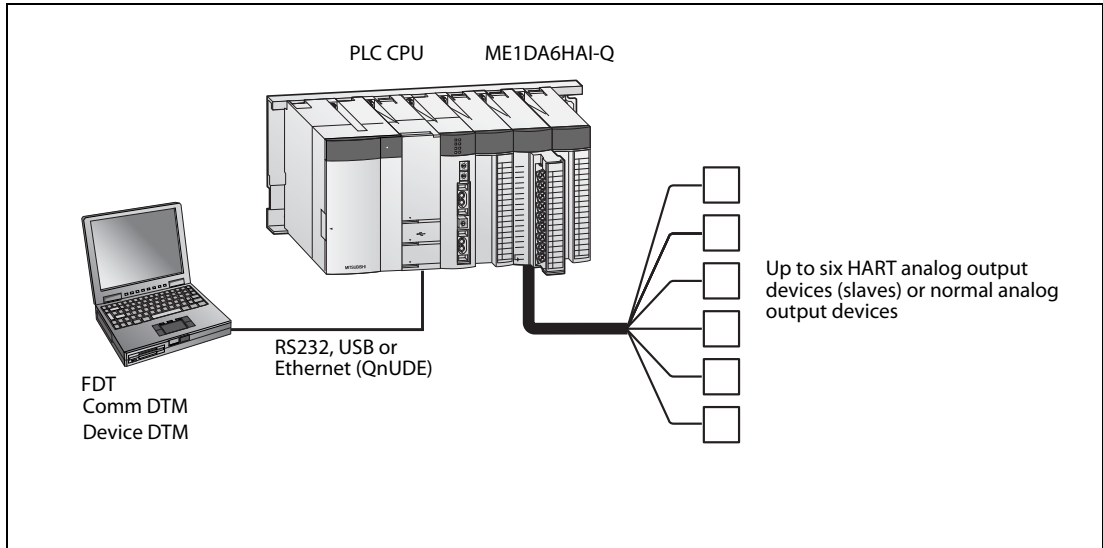
Setting value for switch 4: 0000H (fixed)

Setting value for switch 5: 0000 0000 0001 0001 = 0011H

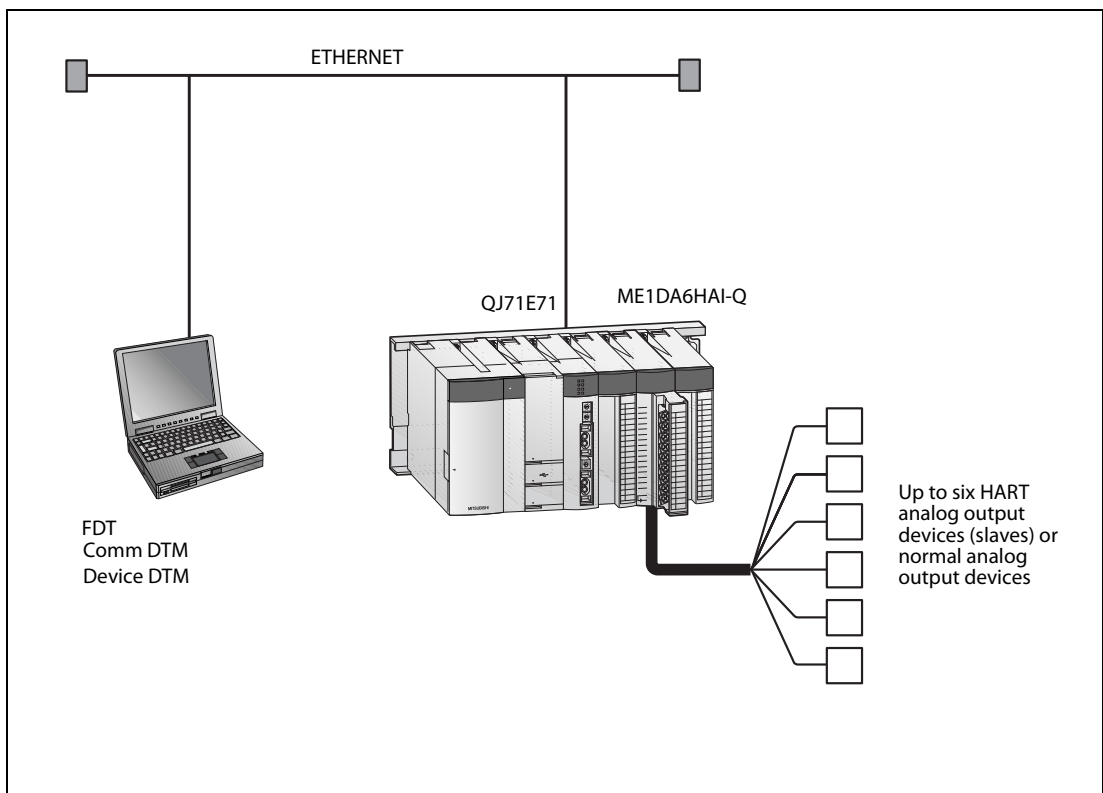
## 4.6 Setting of the HART Devices

For setting the parameters and monitoring the status of HART devices, MX CommDTM-HART can be used.

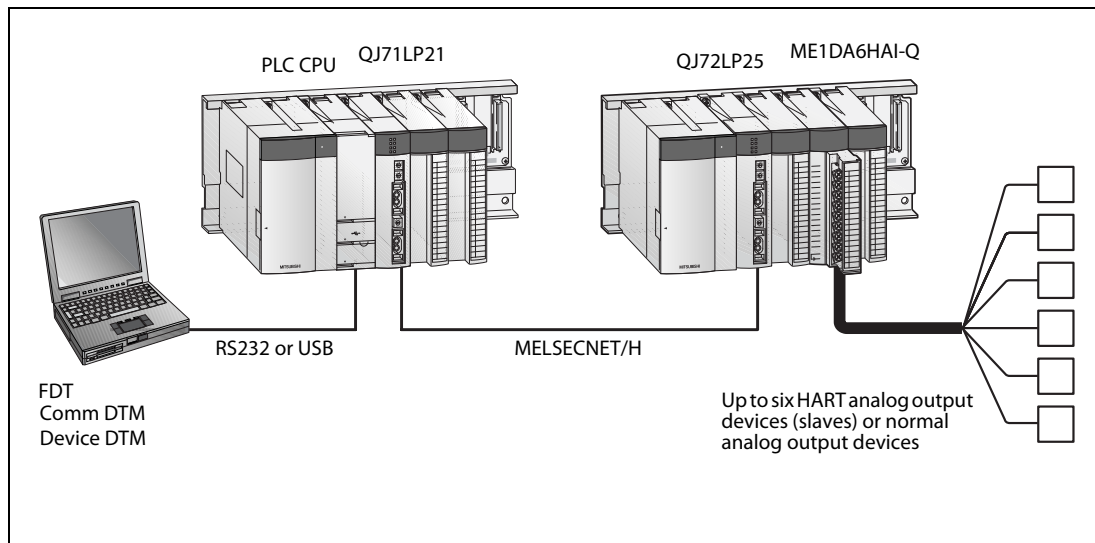
It supports serial CPU port connection (RS-232, USB, Ethernet via QnUDE) as well as Ethernet modules and MELSEC networks.



**Fig. 4-8:** System configuration for the connection of MX CommDTM-HART to the PLC CPU



**Fig. 4-9:** System configuration for the Ethernet connection of MX CommDTM-HART



**Fig. 4-10:** Connection of MX CommDTM-HART via MELSECNET/H

- CommDTM for ME1DA6HAI-Q

It can be downloaded from the following web-site:

[http://www.mitsubishi-automation.com/mymitsubishi\\_index.html](http://www.mitsubishi-automation.com/mymitsubishi_index.html)

Menu "MyMitsubishi" → (Login) → "Downloads" → "Tools"

- Device DTM for each HART device

Please ask the manufacturer of the HART device.



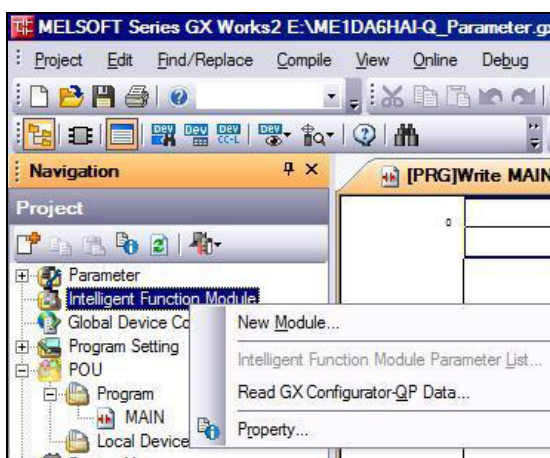
# 5 Intelligent Function Utility (GX Works2)

The programming software GX Works2 allows the quick and easy parameter setting for intelligent function modules like the ME1DA6HAI-Q.

Programming is reduced because the initial setting and automatic data exchange between PLC CPU and ME1DA6HAI-Q can be configured on the screen. In addition, the "switches" of intelligent function modules can be set easily.

## 5.1 Addition of a new Module to the Project

To add a new intelligent function module to a project, click on **Intelligent Function Module** in the Project Navigation window. After a right click, select **New Module**.



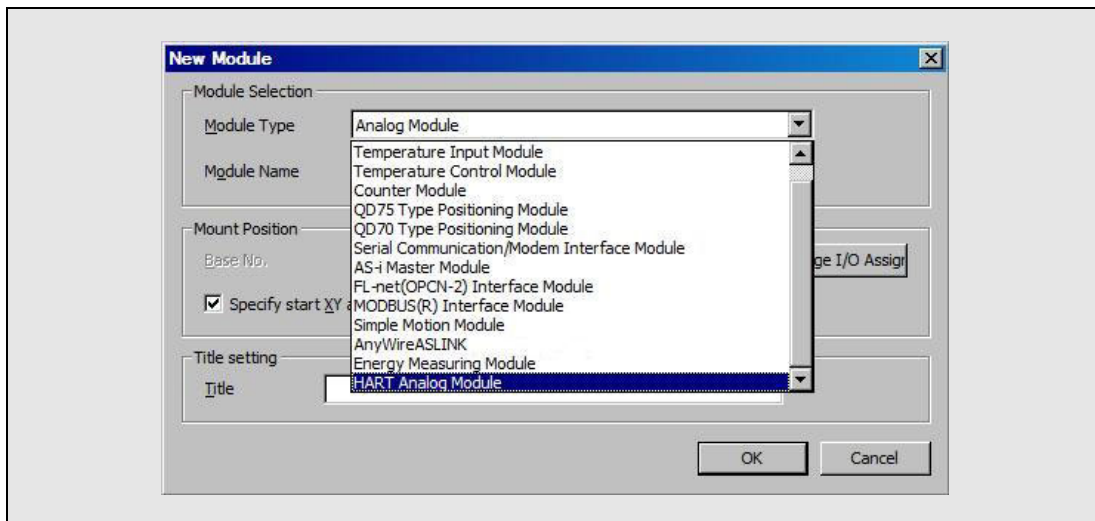
**Fig. 5-1:** Addition of a new intelligent function module

The window **New Module** is displayed.



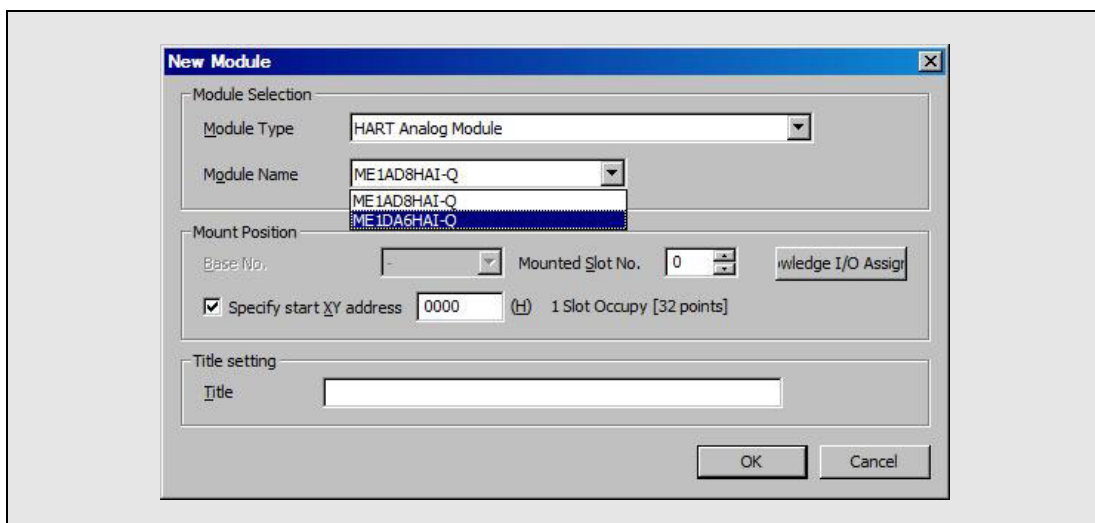
**Fig. 5-2:** Selection of an intelligent function module

Select **HART Analog Module**.



**Fig. 5-3:** Selection of the HART modules

Afterwards, select **ME1DA6HAI-Q**.

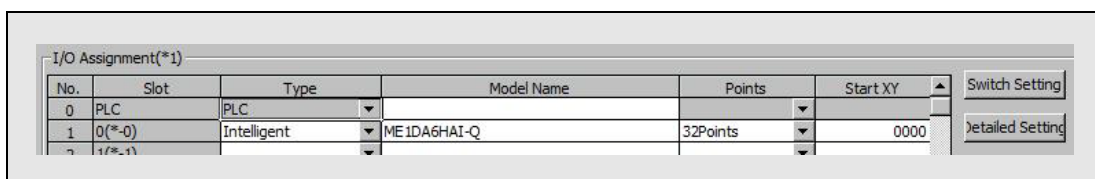


**Fig. 5-4:** Selection of the ME1DA6HAI-Q

Enter the slot No. where the module is mounted (**Mounted Slot No.**) and the start I/O number. As **Title** you can, for instance, enter an individual name for the module. This name is then displayed in the Project Navigation window.

Afterwards click on **OK**.

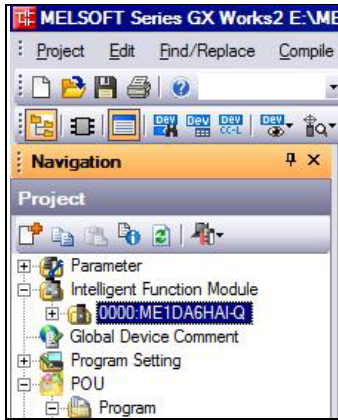
The settings are reflected in the PLC parameters automatically. An I/O assignment (section 4.5.1) there is no longer required.



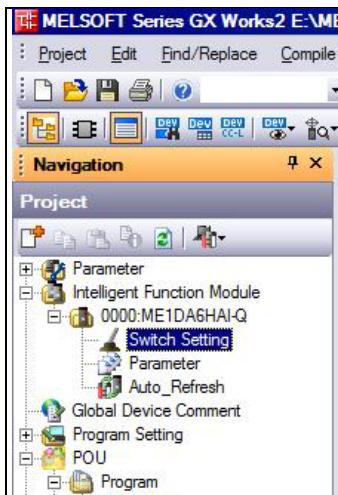
**Fig. 5-5:** Display of the I/O assignment in the PLC parameters

## 5.2 Switch Setting

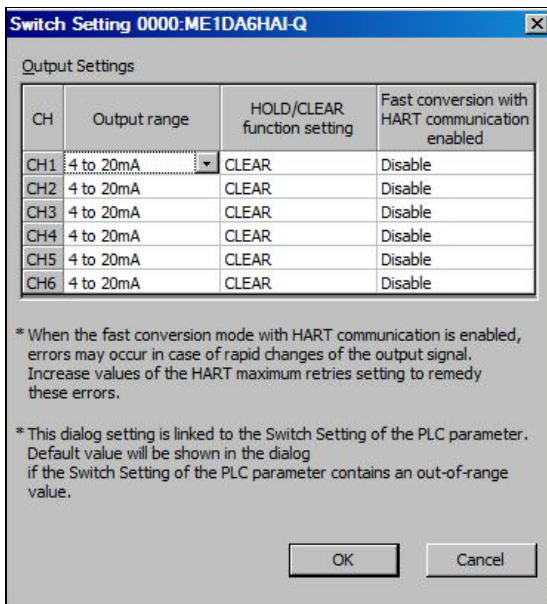
The "switches" of intelligent function modules, otherwise set in the PLC parameters (refer to section 4.5.2), can be set very clearly with GX Works2.



**Fig. 5-6:**  
In the Project Navigation window, click on the plus sign in front of the module name in order to show the setting options.



**Fig. 5-7:**  
Double-click on **Switch Setting**.

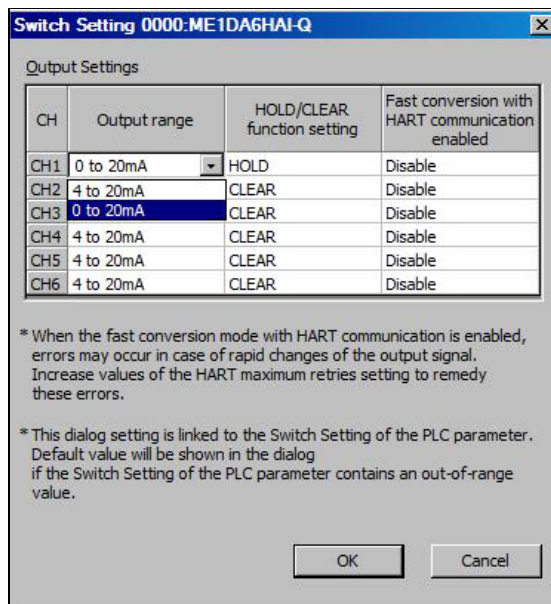


**Fig. 5-8:**  
In this dialog box the output range of each channel and other options can be set.

**Setting options**

- Output range  
0 to 20 mA or 4 to 20 mA
- HOLD/CLEAR function setting  
Holding or clearing of the output value when the PLC CPU is stopped.
- Fast conversion with HART communication enabled  
The fast conversion mode can be disabled or enabled.

The settings are described in detail in section 4.5.2.



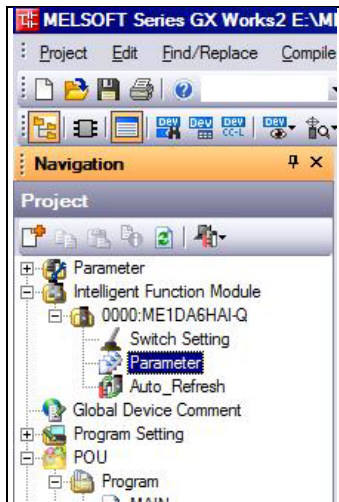
**Fig. 5-9:** Select the desired output range and the options and click on **OK** afterwards.

The settings are reflected in the PLC parameters automatically. Therefore switch setting is no longer required there.

Slot	Type	Model Name	Switch1	Switch2	Switch3	Switch4	Switch5	
0	PLC							
1	0(*-0)	Intelligent	ME1DA6HAI-Q	0001	0000	0001	0000	0000
2	1(*-1)							

**Fig. 5-10:** Display of the switch settings in the PLC parameters

### 5.3 Parameter Setting



**Fig. 5-11:** Double-click on **Parameter**.

0000:ME1DA6HAI-Q]-Par...

Display Filter: Display All

Item	CH1	CH2	CH3	CH4	CH5	CH6
<b>Scaling function</b>						
Set about the scaling of D/A conversion.						
Scaling enable/disable	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable
Scaling upper limit value	0	0	0	0	0	0
Scaling lower limit value	1:Disable	0	0	0	0	0
<b>Rate control function</b>						
Set about the rate control of D/A conversion.						
Rate control enable/disable setting	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable
Increase digital limit value	32000	32000	32000	32000	32000	32000
Decrease digital limit value	32000	32000	32000	32000	32000	32000
<b>Warning output function</b>						
Set about the warning of D/A conversion.						
Warning output setting	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable
Warning output upper limit value	0	0	0	0	0	0
Warning output lower limit value	0	0	0	0	0	0
<b>Circuit control function</b>						
Set about the detection of electrical connections malfunction.						
Short circuit detection setting	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable
Disconnection detection setting	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable	1:Disable
<b>HART function</b>						
Set about HART communication.						
HART enable/disable setting	0:Disable	0:Disable	0:Disable	0:Disable	0:Disable	0:Disable
HART maximum retries	3	3	3	3	3	3
HART device information refresh interval	30 s					

**Fig. 5-12:** Dialog box for parameter setting

Double-click an item to change the setting. Depending on the type of item this action displays a pull-down list with options to choose from or a setting value can be entered directly.

The individual settings are shown on the next page.

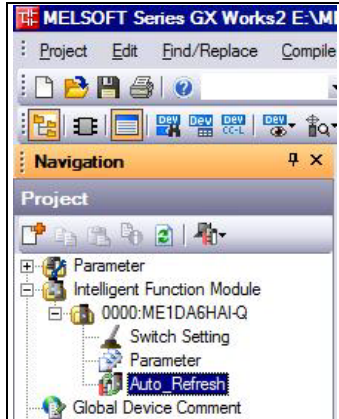
Item		Reference (section)
Scaling function	Scaling enable/disable setting	3.5.12
	Scaling upper limit value	3.5.13
	Scaling lower limit value	
Rate control function	Rate control enable/disable setting	3.5.7
	Increase digital limit value	3.5.14
	Decrease digital limit value	
Warning output function	Warning output setting	3.5.8
	Warning output upper limit value	3.5.15
	Warning output lower limit value	
Circuit control function	Short circuit detection function	3.5.6
	Disconnection detection setting	3.5.8
HART function	HART enable/disable setting	3.5.16
	HART maximum retries	3.5.19
	HART device information refresh interval	3.5.20

**Tab. 5-1:** Adjustable parameter of the ME1DA6HAI-Q

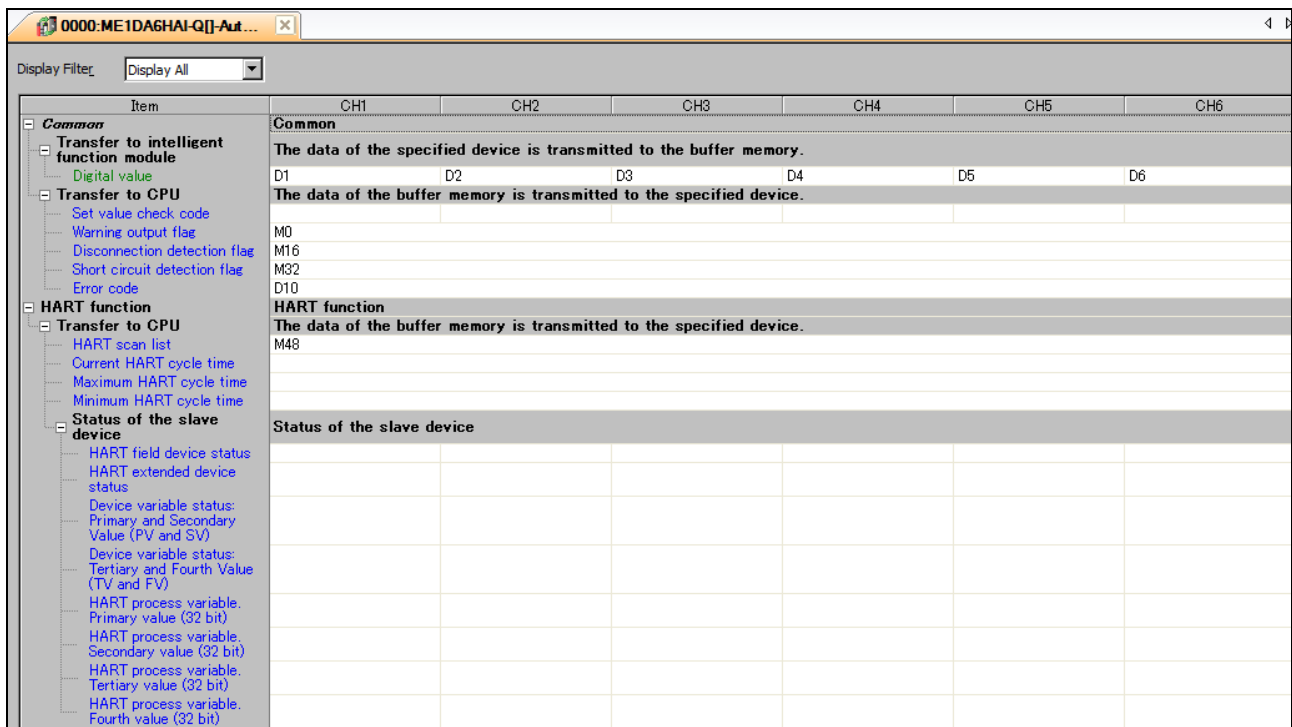
## 5.4 Auto Refresh Settings

Data in the device memory of the PLC CPU can be transferred to the buffer memory of the analog output module or moved from the analog module to the PLC CPU automatically. By using the auto refresh function, the transfer of this data by the sequence program is unnecessary.

The buffer memory that was set for automatic refresh is automatically read or written to when the END command for the programmable controller CPU is executed.



**Fig. 5-13:**  
Double-click on **Auto\_Refresh**



**Fig. 5-14:** Example for the automatic refresh of PLC devices

**NOTES**

Available devices for auto refresh are: X, Y, M, L, B, T, C, ST, D, W, R and ZR.

When a bit device is used, set the head address to "0" or to a value that is divisible by 16 points (example: X10, Y120, M16).

When storing in bit devices, the data in the buffer memory are stored in 16 points of devices from the set device No. (Example: When M16 is set, the data is stored in M16 to M31.)

## 5.5 Writing the Intelligent Function Module Settings to the PLC

When writing the settings for the intelligent function module to the PLC, make sure that the "Intelligent Function Module Parameter" are tagged in the **Online Data Operation** dialog box.

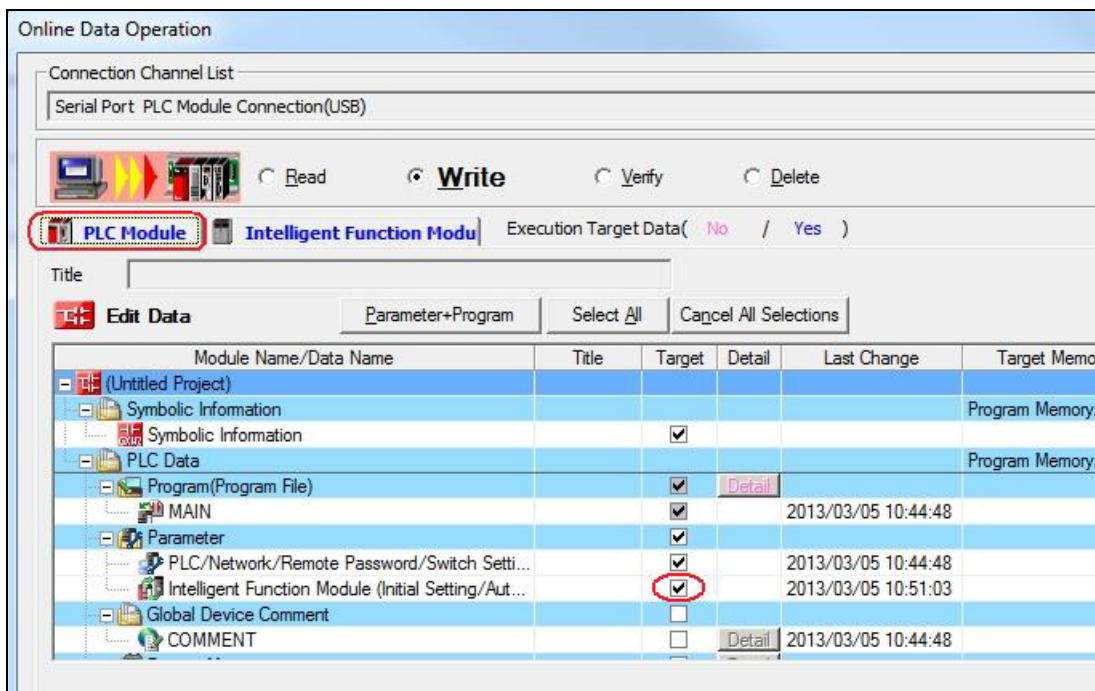


Fig. 5-15: Selection of intelligent function module parameters on the tab "PLC Module"

On the tab "Intelligent Function Module", select the ME1DA6HAI-Q.

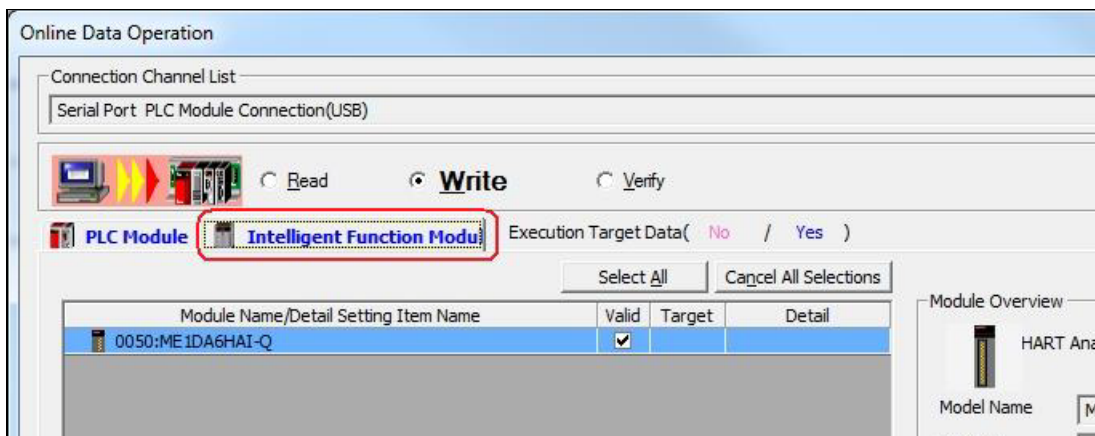


Fig. 5-16: Selection of the HART analog output module



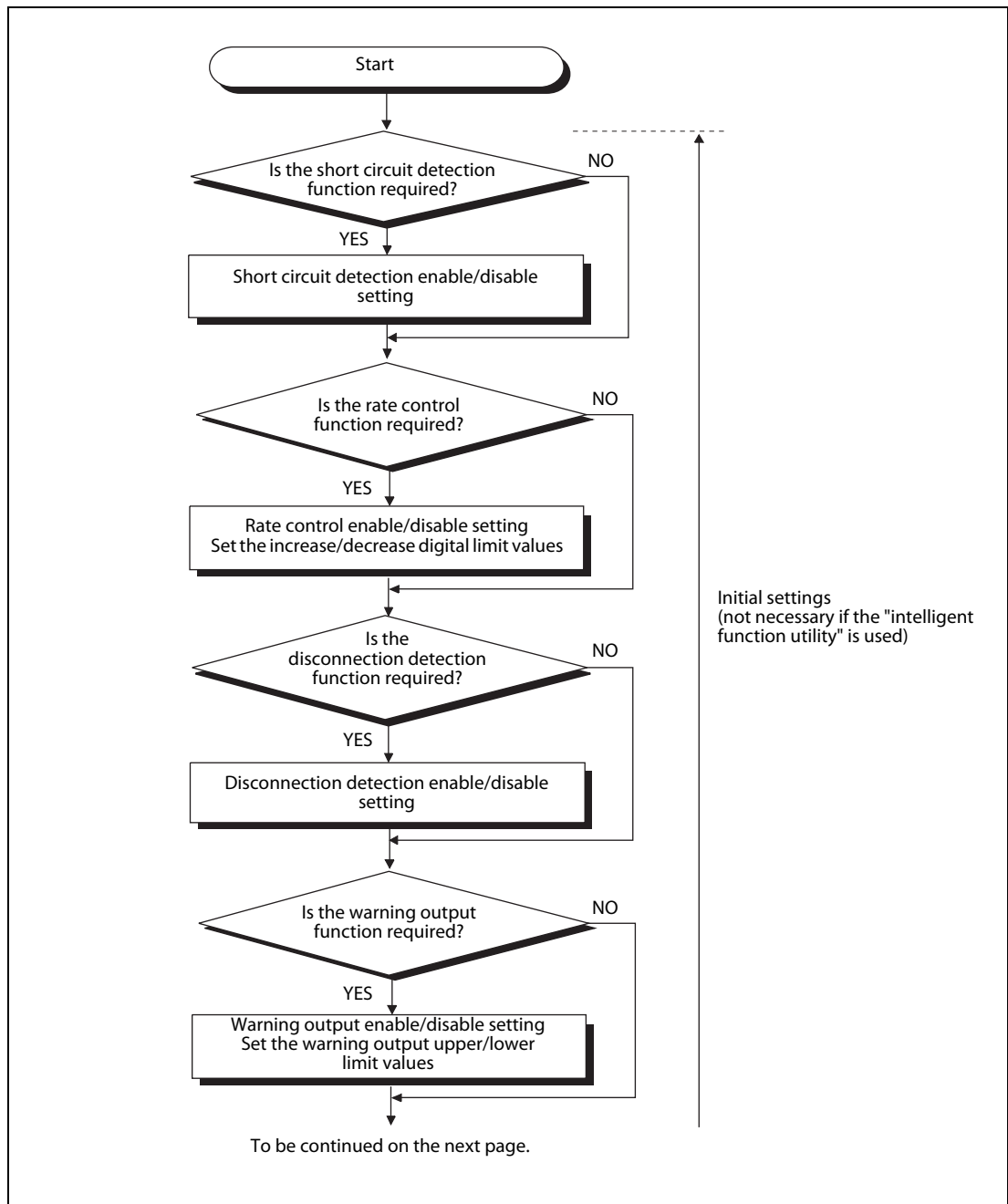
# 6 Programming

This chapter describes the programs of the HART analog output module ME1DA6HAI-Q.

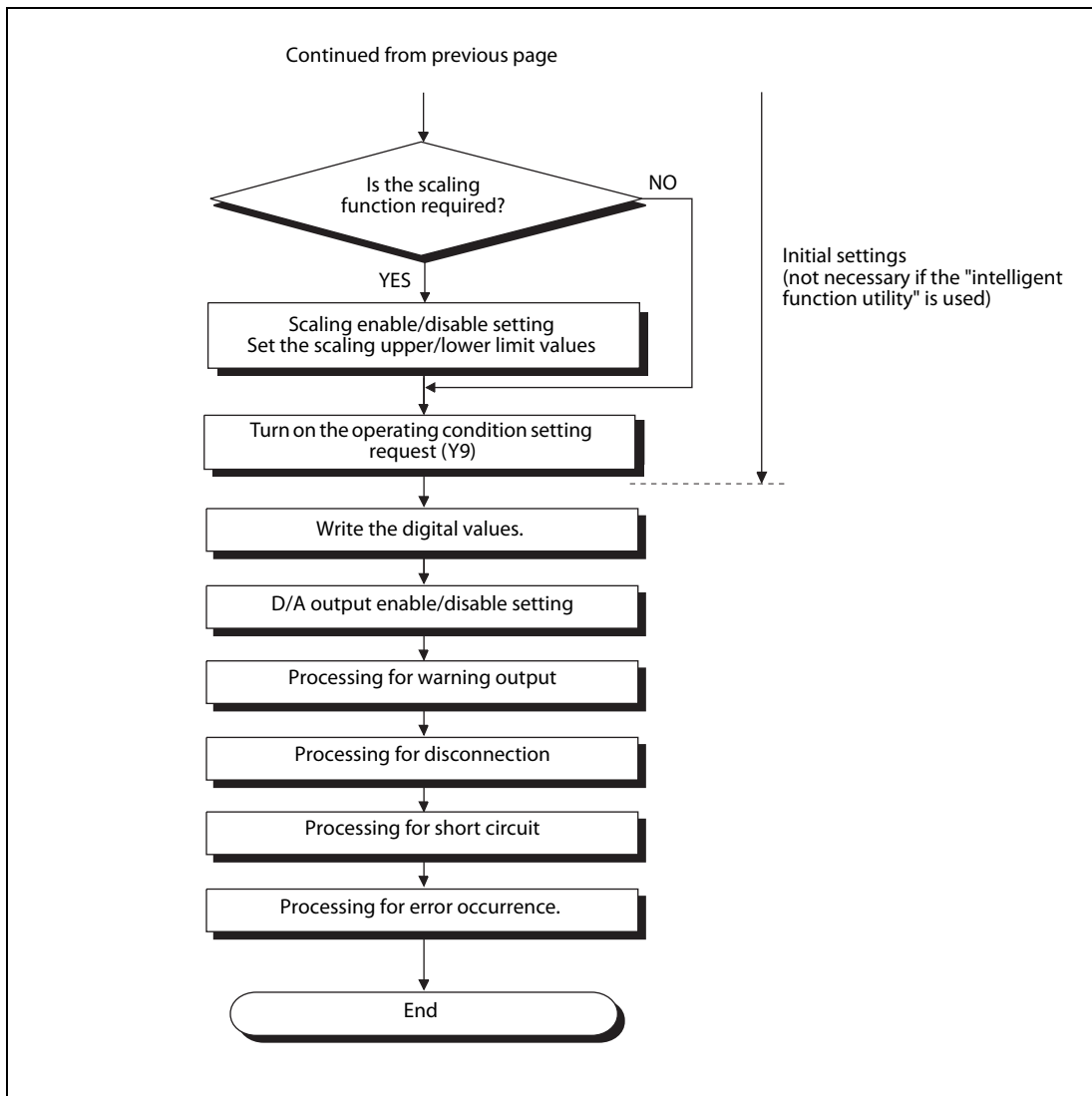
**NOTE** When applying any of the program examples introduced in this chapter to the actual system, verify the applicability and confirm that no problems will occur in the system control.

## 6.1 Programming Procedure

Create a program that will execute the digital-analog conversion of the ME1DA6HAI-Q in the following procedure.



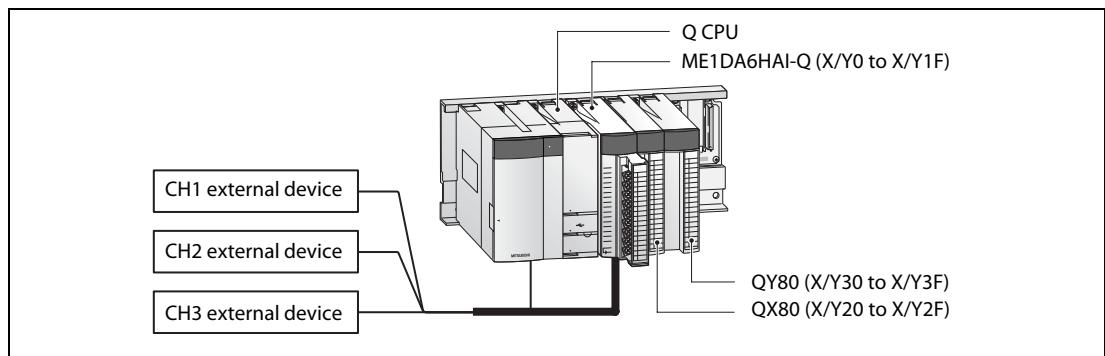
**Fig. 6-1:** Programming procedure for the ME1DA6HAI-Q



**Fig. 6-2:** Programming procedure for the ME1DA6HAI-Q

## 6.2 Example 1: ME1DA6HAI-Q combined with PLC CPU

The following figure shows the system configuration used for this example. Three HART enabled analog devices are connected to a ME1DA6HAI-Q.



**Fig. 6-3:** In this example the ME1DA6HAI-Q is mounted on the main base unit together with an input and an output module.

Channel	Output range setting	HOLD/CLEAR function setting	Fast conversion mode with HART communication enabled
CH1	4 to 20 mA	CLEAR	Disabled
CH2	0 to 20 mA	HOLD	
CH3	4 to 20 mA	CLEAR	
CH4 to CH6	not used	—	—

**Tab. 6-1:** Conditions for the intelligent function module switch setting

### Program conditions

- CH1 uses the rate control function (Refer to section 3.3.3.)
  - CH1 increase digital limit value: 100
  - CH1 decrease digital limit value: 30
- CH2 uses the warning output function (Refer to section 3.3.5.)
  - CH2 warning output upper limit value: 10000
  - CH2 warning output lower limit value: 3000

If a warning is triggered, the warning output flag status is read and processing for the warning output is performed.

- CH3 uses the scaling function (Refer to section 3.3.4)
  - CH3 scaling upper limit value: 20000 (equals 20 mA)
  - CH3 scaling lower limit value: 4000 (equals 4 mA)
- Disconnection detection is enabled for CH1 and CH3.

In case of a disconnection, the disconnection detection flag status is read and processing for the disconnection is performed.

- Short circuit detection is enabled for CH1 and CH3.

When a short circuit occurs, the short circuit detection flag status is read and processing for the short circuit is performed.

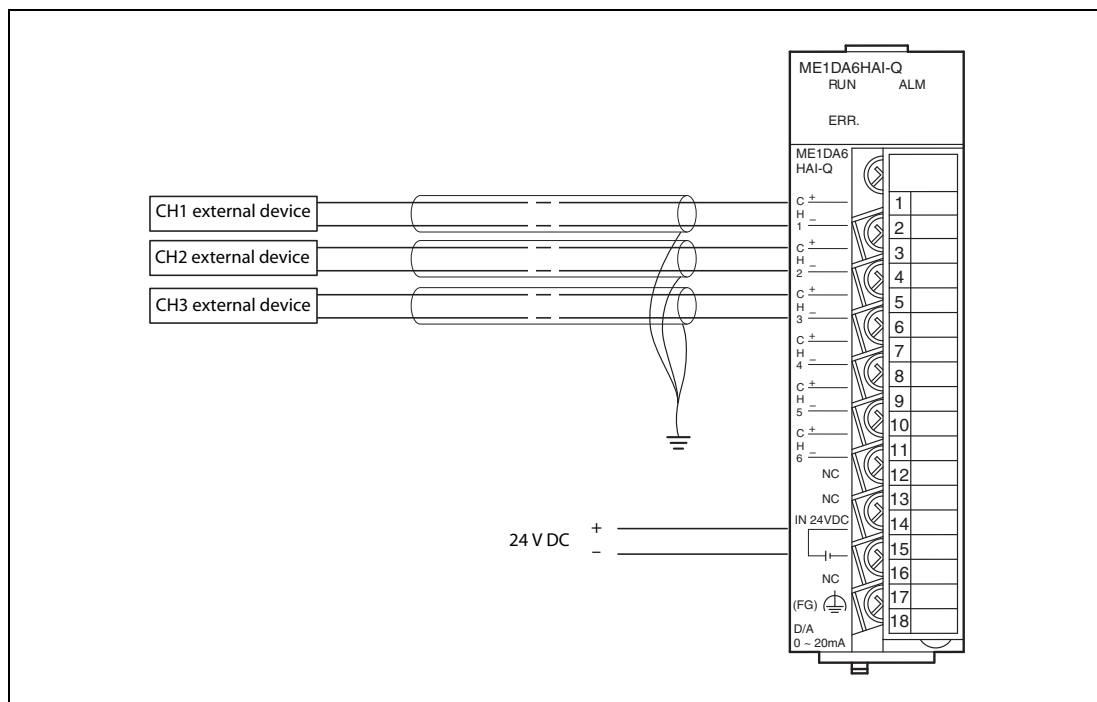
- In the event of an error, the error code shall be displayed in BCD format. The error code shall be reset after removal of the cause.
- A warning lamp for each channel is switched ON if the connected device is malfunctioning.

### 6.2.1 Before creating a program

Perform the following steps before creating a program.

#### Wiring of external devices

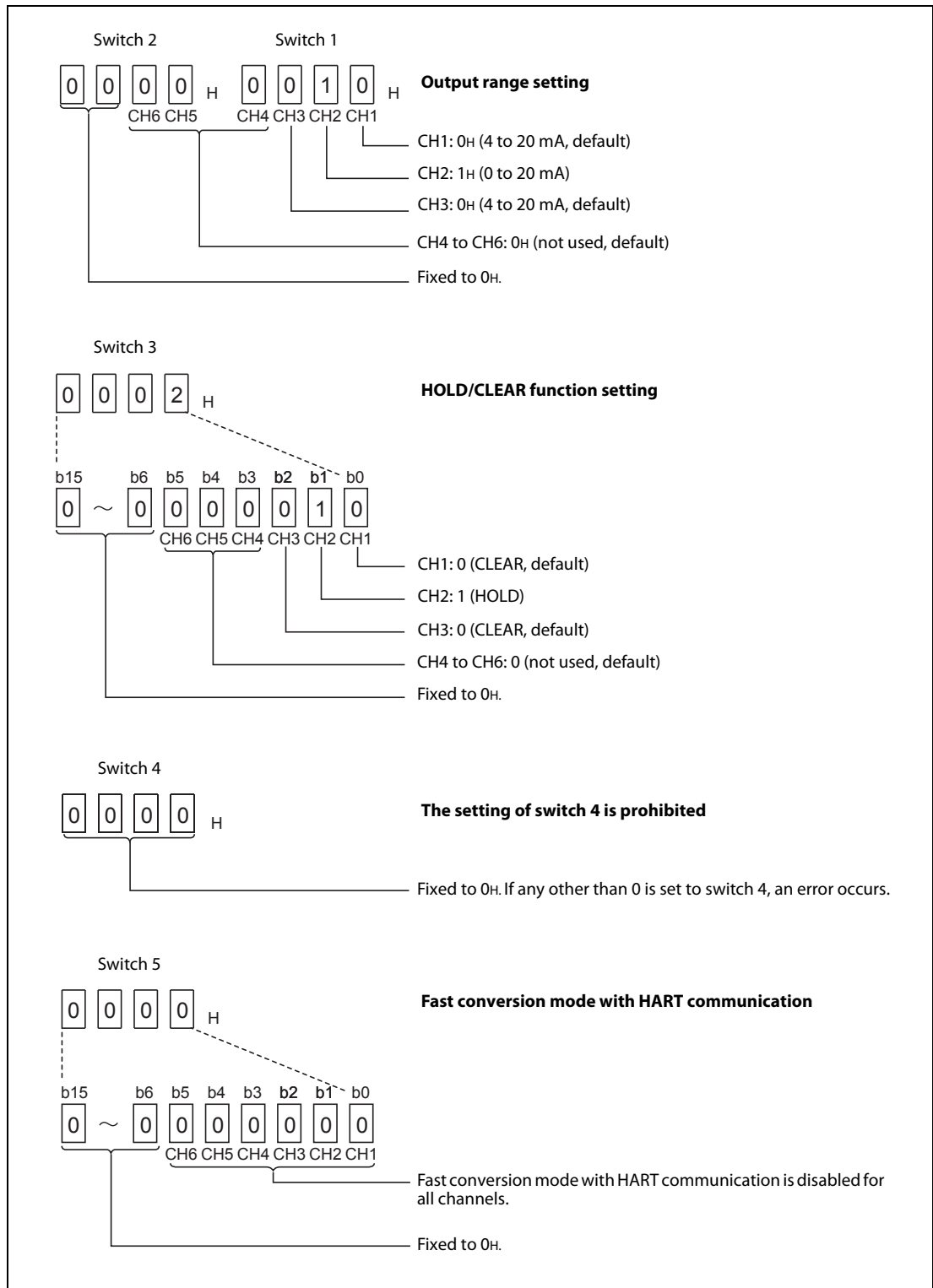
Mount the ME1DA6HAI-Q on the base unit and connect the external power supply and the external devices. For details, refer to section 4.4.



**Fig. 6-4:** External wiring required for this example

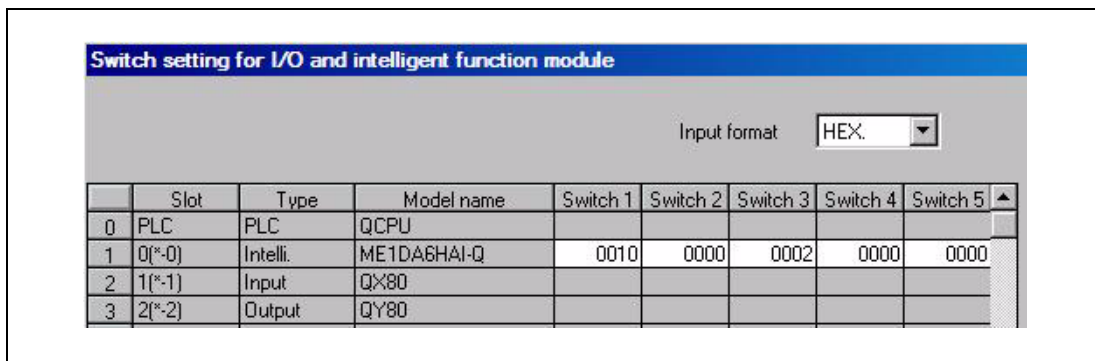
**Intelligent function module switch setting**

Based on the setting conditions given previously, make the intelligent function module switch settings.



**Fig. 6-5:** Setting of the switches 1 to 5 for this example

On GX Developer's or GX IEC Developer's **Parameter setting** screen, select the **I/O assignment** tab, click **Switch setting**, and make settings of the switches 1 to 5 as on the screen shown below (for details about the setting, refer to section 4.5.2).



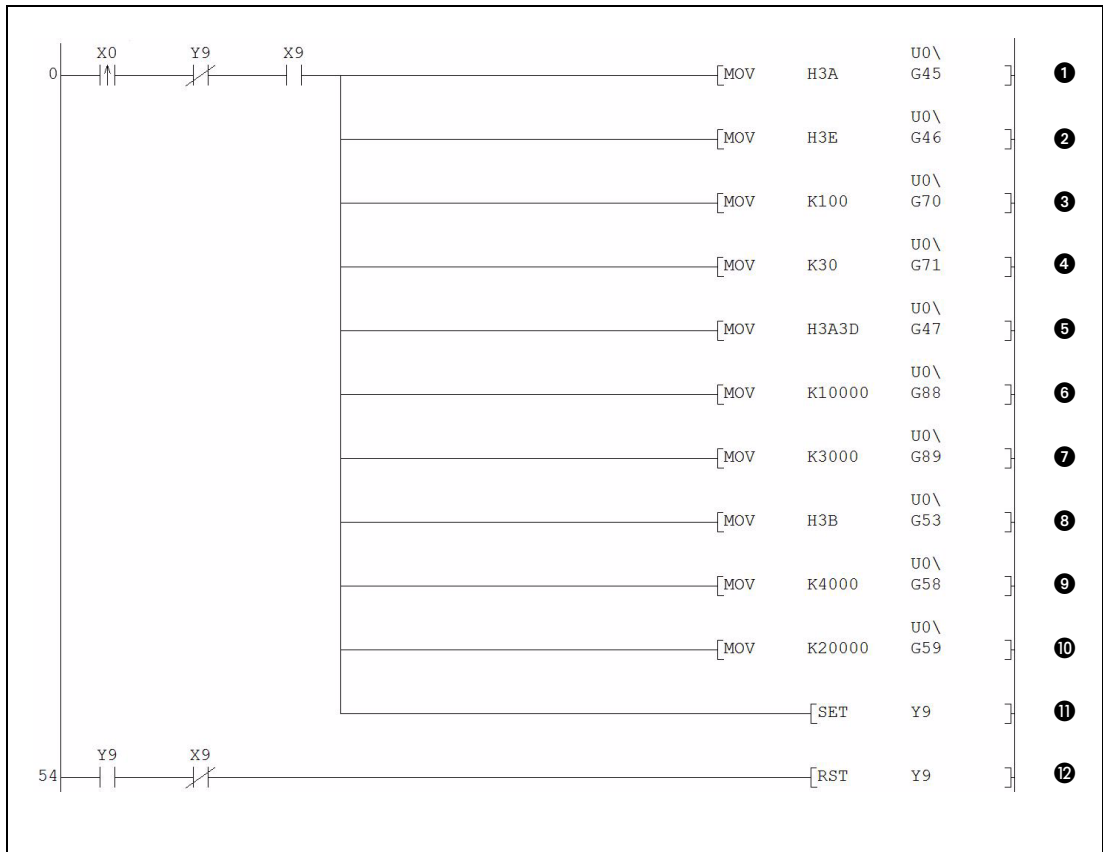
**Fig. 6-6:** Switch setting for this example

**6.2.2 Program**

Device	Function	Remark	
Inputs	X0	Module ready	ME1DA6HAI-Q (X0 to X1F)
	X9	Operating condition setting completed flag	
	XD	Disconnection detection signal	
	XE	Warning output signal	
	XF	Error flag	
	X10	Short circuit detection signal	
	X20	Output enable	QX80 (X20 to X2F)
	X21	Digital value write signal	
	X22	Warning output reset signal	
	X23	Disconnection detection reset signal	
	X24	Short circuit reset signal	
	X25	Error code reset signal	
	X26	CH1 HART device communication request	
	X27	CH2 HART device communication request	
X28	CH3 HART device communication request		
Outputs	Y1	CH1 output enable	ME1DA6HAI-Q (Y0 to Y1F)
	Y2	CH2 output enable	
	Y3	CH3 output enable	
	Y9	Operating condition setting request	
	YE	Warning output clear request	
	YF	Error clear request	
	Y10	Short circuit detection clear request	QY80 (Y30 to Y3F)
	Y30 to Y3B	Error code display (BCD 3 digits)	
	Y3C	Warning lamp: CH1 output device malfunction	
	Y3D	Warning lamp: CH2 output device malfunction	
Y3F	Warning lamp: CH3 output device malfunction		
Internal relays	M12	CH2 Warning output flag (Upper limit)	The warning output flags for all channels are stored in M10 to M21.
	M13	CH2 Warning output flag (Lower limit)	
	M30	CH1 Disconnection detection flag	The disconnection detection flags for all channels are stored in M30 (CH1) to M35 (CH6).
	M32	CH3 Disconnection detection flag	
	M40	CH1 Short circuit detection flag	The short circuit detection flags for all channels are stored in M40 (CH1) to M45 (CH6).
	M42	CH3 Short circuit detection flag	
	M100 M101 M102	HART device found at CH1, CH2 and CH3	M100 to M105 are set when a HART device is detected at the channels 1 to 6.
	M117	CH1 device malfunction	M110 to M117: Status of HART field device connected to CH1
	M127	CH2 device malfunction	M120 to M127: Status of HART field device connected to CH2
M137	CH3 device malfunction	M130 to M137: Status of HART field device connected to CH3	
Register	D1	CH1 Digital value	
	D2	CH2 Digital value	
	D3	CH3 Digital value	

**Tab. 6-2:** List of used devices

● Initial settings



**Fig. 6-7:** The initial settings are performed once when X0 (Module ready) turns on.

Number	Description
①	Short circuit detection enable/disable setting (CH1, CH3: enable)
②	Rate control enable/disable setting (CH1: enable)
③	Rate control: Setting of the CH1 increase digital limit value
④	Rate control: Setting of the CH1 decrease digital limit value
⑤	The following settings are written to the buffer memory address U0\G47: <ul style="list-style-type: none"> <li>• High byte: Disconnection detection enable/disable setting (CH1, CH3: enable)</li> <li>• Low byte: Warning output enable/disable setting (CH2: enable)</li> </ul>
⑥	CH2 warning output setting: Upper limit value
⑦	CH2 warning output setting: Lower limit value
⑧	Scaling enable/disable setting (CH3: enable)
⑨	Setting of the CH3 scaling lower limit value
⑩	Setting of the CH3 scaling upper limit value
⑪	The operation condition setting request (Y9) is turned ON.
⑫	When the setting is completed, the operation condition setting request is turned OFF.

**Tab. 6-3:** Description of the program for the initial settings



● Communication with HART devices

The following part of the program is optional. If the HART devices are set and monitored with the tool MX CommDTM-HART, these instructions can be omitted.

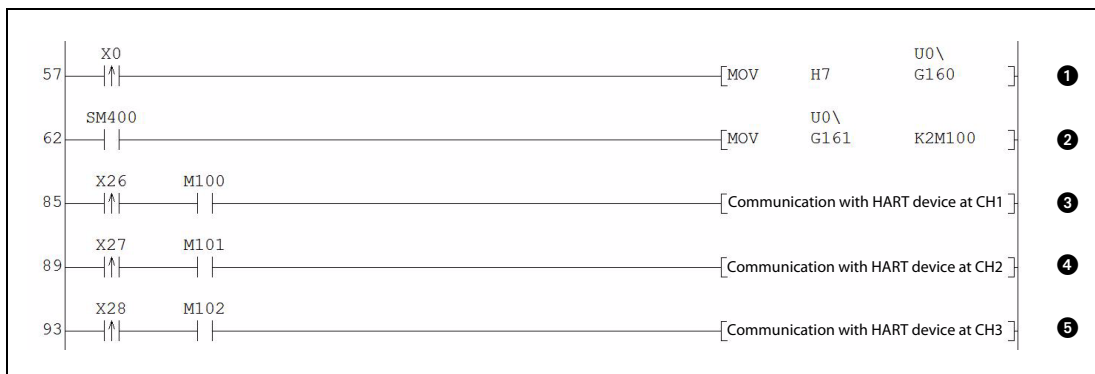


Fig. 6-8: Communication with HART devices

Number	Description	
①	HART enable/disable setting (CH1, CH2, CH3: HART enabled)	
②	The HART scan list is moved to the internal relays M100 to M107. Since SM400 is always ON, this MOV instruction is executed in every program cycle.	
③	Sending of commands to the HART device, reading of information received from the HART device etc.	CH1
④		CH2
⑤		CH3

Tab. 6-4: Description of the program shown above

● Writing of digital values and analog output enable setting

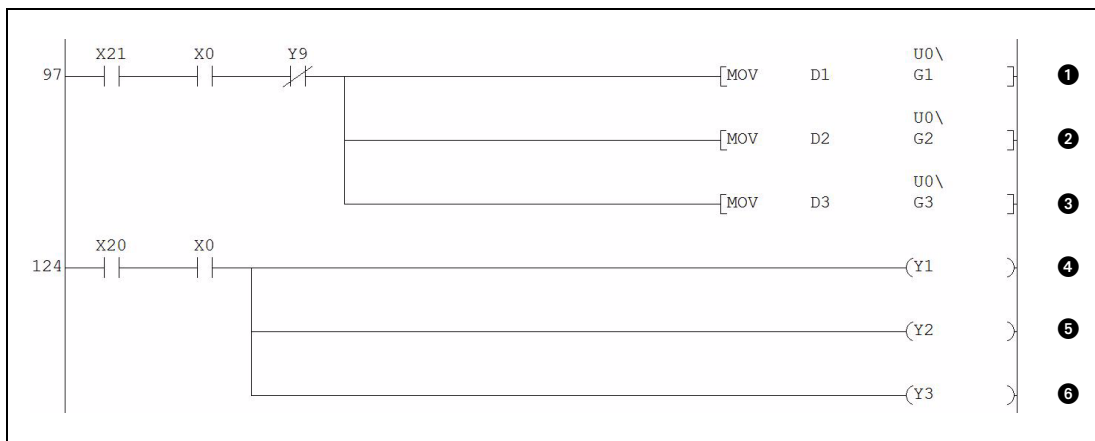


Fig. 6-9: The digital values are stored in the registers D1 to D3.

Number	Description	
①	The digital values are moved from the registers where they were temporary stored by instructions elsewhere in the program to the corresponding buffer memory addresses.	CH1
②		CH2
③		CH3
④	The analog output is enabled.	CH1
⑤		CH2
⑥		CH3

Tab. 6-5: Description of the program shown above

● Warning occurrence status and processing at warning occurrence

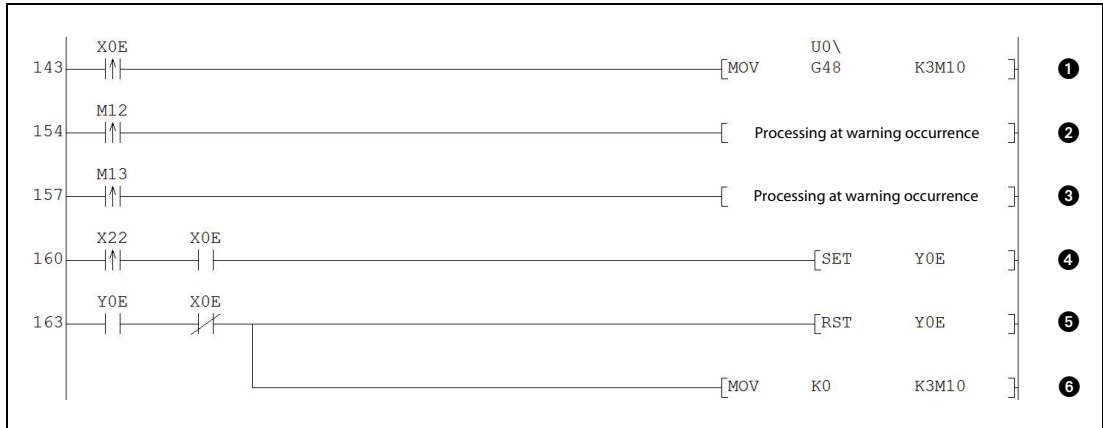


Fig. 6-10: Program part for warning processing

Number	Description	
①	When the warning output signal (X0E) is ON, the status of the warning output flags is moved to the internal relays M10 to M21.	
②	Processing at warning occurrence	CH2 upper limit value warning
③		CH2 lower limit value warning
④	When X22 (Warning output reset signal) is switched ON while the warning output signal is ON, the warning output clear request (Y0E) is turned ON.	
⑤	When there is no warning indicated, the warning output clear request (Y0E) is turned OFF.	
⑥	The internal relays storing the warning output flags are also cleared.	

Tab. 6-6: Description of the program shown above

● Disconnection detection status and processing at disconnection detection

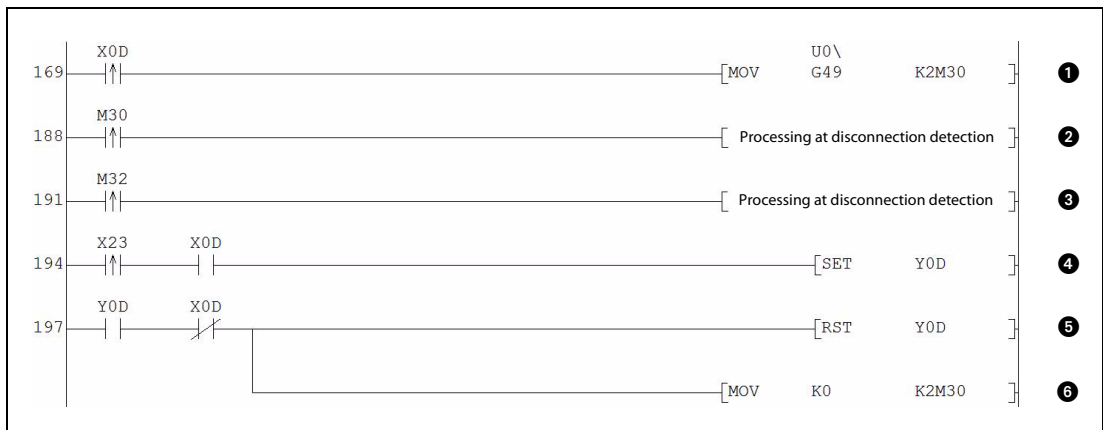


Fig. 6-11: Sequence program for disconnection detection

Number	Description	
①	When the disconnection detection signal (X0D) is ON, the status of the disconnection detection flags is moved to the internal relays M30 to M35.	
②	Processing at disconnection detection	CH1
③		CH3
④	When X23 (Disconnection detection reset signal) is switched ON while the disconnection detection signal is ON, the disconnection detection clear request (Y0D) is turned ON.	
⑤	When there is no disconnection indicated, the disconnection detection clear request (Y0D) is turned OFF.	
⑥	The internal relays storing the disconnection detection flags are also cleared.	

Tab. 6-7: Description of the program shown above

● Short circuit detection status and processing at short circuit detection

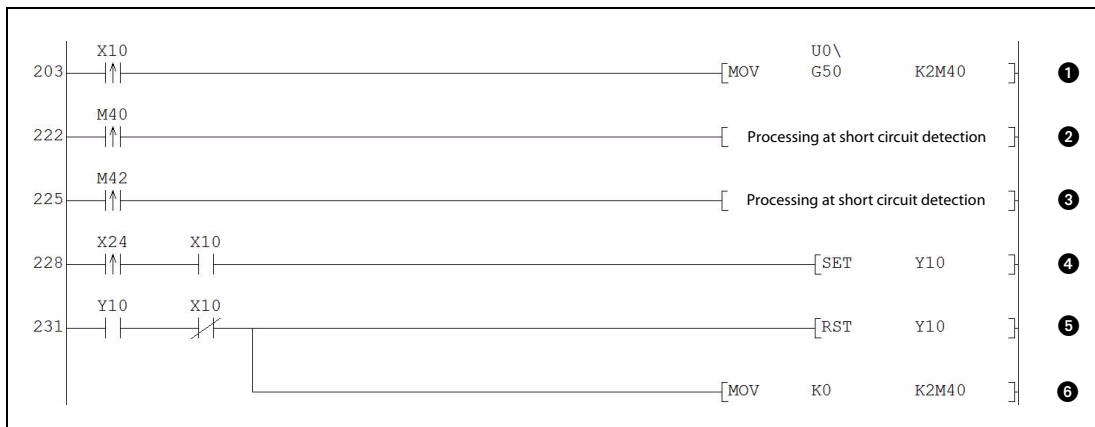


Fig. 6-12: Sequence program for short circuit detection

Number	Description	
①	When the short circuit detection signal (X10) is ON, the status of the short circuit detection flags is moved to the internal relays M40 to M45.	
②	Processing at short circuit detection	CH1
③		CH3
④	When X24 (Short circuit detection reset signal) is switched ON while the short circuit detection signal is ON, the short circuit detection clear request (Y10) is turned ON.	
⑤	When there is no short circuit indicated, the short circuit detection clear request (Y10) is turned OFF.	
⑥	The internal relays storing the short circuit detection flags are also cleared.	

Tab. 6-8: Description of the program shown above

● Error detection and display

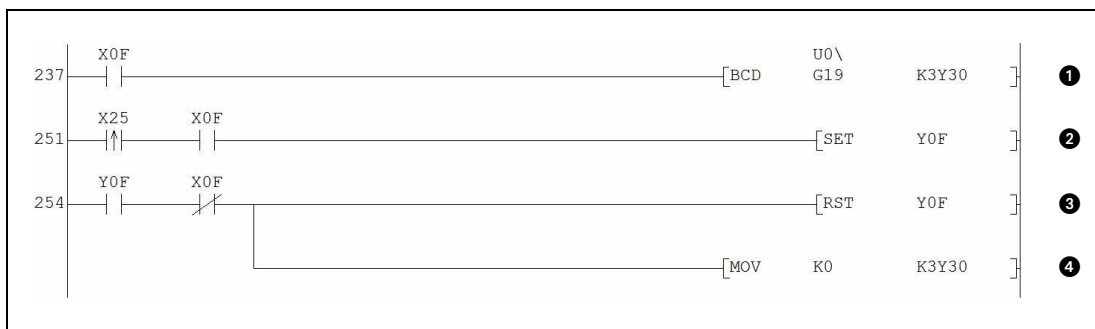


Fig. 6-13: Error detection, display and handling

Number	Description
①	In case of an error the error code is output in BCD.
②	When an error has been detected and the reset signal (X25) is ON, the error clear request (Y0F) is set.
③	When there is no error indicated, the error clear request (Y0F) is turned OFF.
④	The error code outputs are also cleared.

Tab. 6-9: Description of the program shown above

● HART field device status check and processing at device malfunction

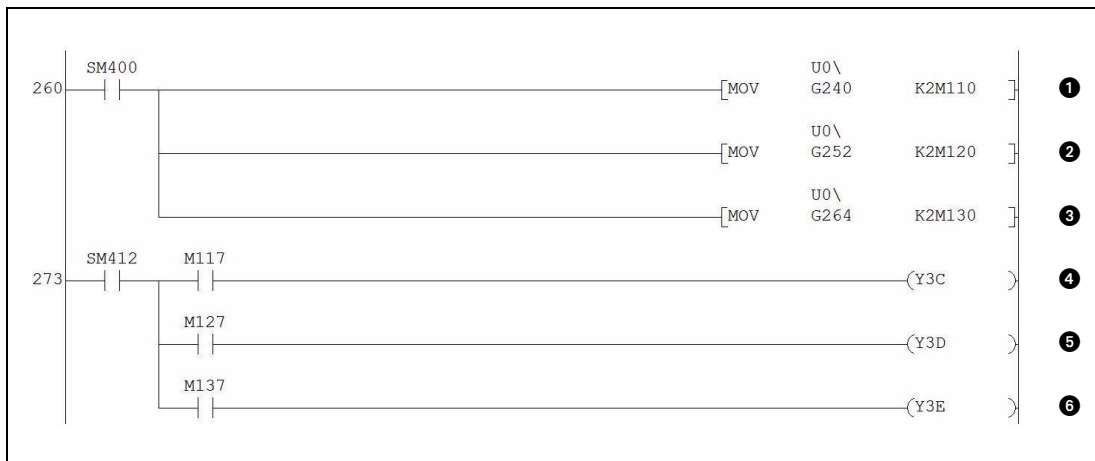


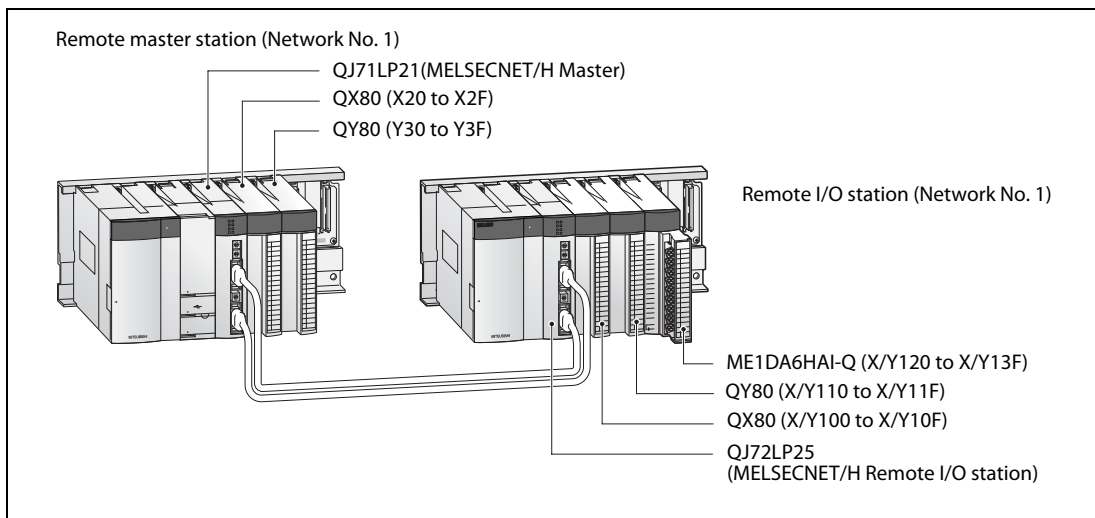
Fig. 6-14: HART field device status check and error processing

Number	Description
1	The HART field device status is read and stored in internal relays (These MOV instructions are executed in every program cycle since SM400 is always ON.).
2	Status of device connected to CH1
3	Status of device connected to CH2
4	Status of device connected to CH3
5	Device malfunction at CH1
6	Device malfunction at CH2
	Device malfunction at CH3

Tab. 6-10: Description of the program shown above

### 6.3 Example 2: ME1DA6HAI-Q used in Remote I/O Network

#### System configuration



**Fig. 6-15:** For this example the ME1DA6HAI-Q is installed in a remote I/O station.

Channel	Output range setting	HOLD/CLEAR function setting
CH1	4 to 20 mA	CLEAR
CH2	0 to 20 mA	HOLD
CH3	4 to 20 mA	CLEAR
CH4 to CH6	not used	—

**Tab. 6-11:** Conditions for the intelligent function module switch setting

#### Program conditions

- CH1 uses the rate control function (Refer to section 3.3.3.)
  - CH1 increase digital limit value: 100
  - CH1 decrease digital limit value: 30
- CH2 uses the warning output function (Refer to section 3.3.5.)
  - CH2 warning output upper limit value: 10000
  - CH2 warning output lower limit value: 3000

If a warning is triggered, the warning output flag status is read and processing for the warning output is performed.

- CH3 uses the scaling function (Refer to section 3.3.4)
  - CH3 scaling upper limit value: 20000
  - CH3 scaling lower limit value: 4000
- Disconnection detection is enabled for CH1 and CH3.

In case of a disconnection, the disconnection detection flag status is read and processing for the disconnection is performed.

- Short circuit detection is enabled for CH1 and CH3.

When a short circuit occurs, the short circuit detection flag status is read and processing for the short circuit is performed.

- In the event of an error, the error code shall be displayed in BCD format.

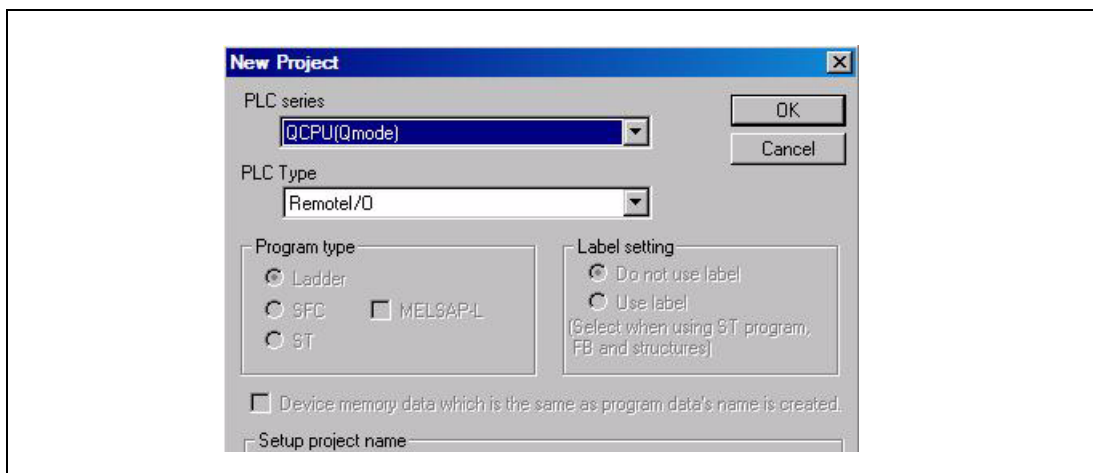
The error code shall be reset after removal of the cause.

- If one of the connected HART device is malfunctioning, error processing is performed.

### 6.3.1 Before creating a program

Before creating the program, perform the steps described in section 6.2.1.

The PLC parameters for a remote I/O module can be set in the same manner as for the CPU module. However, for a remote I/O station only the required items can be set.



**Fig. 6-16:** When creating a project for a remote I/O station, select "Remote I/O" as PLC Type.

To write the intelligent function module parameters, set the target remote I/O station from the Online menu (Transfer setup) on GX Developer or GX IEC Developer. They can be written by:

- Directly connecting GX (IEC) Developer to the remote I/O station.
- Connecting GX (IEC) Developer to another device such as a CPU module and passing through the network.

#### List of devices

Device	Function	Remark	
Inputs (in main base unit)	X20	Output enable	QX80 (X20 to X2F)
	X21	Digital value write signal	
	X22	Warning output reset signal	
	X23	Disconnection detection reset signal	
	X24	Short circuit reset signal	
	X25	Error code reset signal	
	X26	CH1 HART device communication request	
	X27	CH2 HART device communication request	
	X28	CH3 HART device communication request	
X2F	Initial setting request signal		
Inputs (in remote I/O station)	X120	Module ready	ME1DA6HAI-Q (X120 to X13F)
	X129	Operating condition setting completed flag	
	X12D	Disconnection detection signal	
	X12E	Warning output signal	
	X12F	Error flag	
X130	Short circuit detection signal		
Outputs (in main base unit)	Y30 to Y3B	Error code display (BCD 3 digits)	QY80 (Y30 to Y3F)

**Tab. 6-12:** List of used devices

Device	Function	Remark		
Outputs (in remote I/O station)	Y121	CH1 output enable	ME1DA6HAI-Q (Y120 to Y13F)	
	Y122	CH2 output enable		
	Y123	CH3 output enable		
	Y129	Operating condition setting request		
	Y12E	Warning output clear request		
	Y12F	Error clear request		
	Y130	Short circuit detection clear request		
Internal relays	M12	CH2 Warning output flag (Upper limit)	The warning output flags for all channels are stored in M10 to M21.	
	M13	CH2 Warning output flag (Lower limit)		
	M30	CH1 Disconnection detection flag	The disconnection detection flags for all channels are stored in M30 (CH1) to M35 (CH6).	
	M32	CH3 Disconnection detection flag		
	M40	CH1 Short circuit detection flag	The short circuit detection flags for all channels are stored in M40 (CH1) to M45 (CH6).	
	M42	CH3 Short circuit detection flag		
	M100 M101 M102	HART device found at CH1, CH2 and CH3	M100 to M105 are set when a HART device is detected at the channels 1 to 6.	
	M117	CH1 device malfunction	M110 to M117: Status of HART field device connected to CH1	
	M127	CH2 device malfunction	M120 to M127: Status of HART field device connected to CH2	
	M137	CH3 device malfunction	M130 to M137: Status of HART field device connected to CH3	
	M200	REMTO instruction is completed normally	REMTO instructions for initial setting of the ME1DA6HAI-Q	
	M201	REMTO instruction is completed with an error		
	M210	REMTO instruction is completed normally		
	M211	REMTO instruction is completed with an error		
	M220	REMTO instruction is completed normally		
	M221	REMTO instruction is completed with an error		
	M230	REMTO instruction is completed normally		
	M231	REMTO instruction is completed with an error		
	M240	REMTO instruction is completed normally		
	M241	REMTO instruction is completed with an error		
	M250	REMTO instruction is completed normally		
	M251	REMTO instruction is completed with an error		
	M260	REMTO instruction is completed normally		REMTO instruction for writing the digital values
	M261	REMTO instruction is completed with an error		
	M300	REMFR instruction is completed normally	REMFR instruction for reading the HART scan list	
	M301	REMFR instruction is completed with an error		
	M310	REMFR instruction is completed normally	REMFR instruction for reading the warnings	
	M311	REMFR instruction is completed with an error		
	M320	REMFR instruction is completed normally	REMFR instruction for reading the disconnection status.	
	M321	REMFR instruction is completed with an error		
	M330	REMFR instruction is completed normally	REMFR instruction for reading the short circuit status.	
	M331	REMFR instruction is completed with an error		
	M340	REMFR instruction is completed normally	REMFR instruction for reading the error code.	
	M341	REMFR instruction is completed with an error		
	M350	REMFR instruction is completed normally	REMFR instruction for reading the status of the HART field device connected to CH1	
	M351	REMFR instruction is completed with an error		
	M360	REMFR instruction is completed normally	REMFR instruction for reading the status of the HART field device connected to CH2	
	M361	REMFR instruction is completed with an error		
	M370	REMFR instruction is completed normally	REMFR instruction for reading the status of the HART field device connected to CH3	
	M371	REMFR instruction is completed with an error		

**Tab. 6-12:** List of used devices

Device	Function	Remark	
Internal relays	M1000	Master control instruction for the processing concerning the ME1DA6HAI-Q	
	M1001	Initial setting of ME1DA6HAI-Q requested	
	M1002	Perform initial setting of ME1DA6HAI-Q	
	M1010	Scanning of HART field device status in progress	
Link Devices	SB20	Module status	
	SB47	Baton pass status (host)	Link status of MELSECNET/H remote master station
	SB49	Host data link status	
	SW70	Baton pass status of each station	Link status of MELSECNET/H remote I/O station (station No. 1)
	SW74	Cyclic transmission status of each station	
SW78	Parameter communication status of each station		
Timer	T100	Baton pass status	Delay for network communication errors.
	T101	Data link status	
	T102	Baton pass status	
	T103	Cyclic transmission status	
	T104	Parameter communication status	
Register	D1 to D161	Temporary storage for the parameters and flags of the ME1DA6HAI-Q. These registers are an image of the corresponding buffer memory addresses.	D1 -> Un\G1, D2 -> Un\G2, D3 -> Un\G3 ..... D161 -> Un\G161
	D240	CH1 Field Device status	Contents of Un\G240
	D252	CH2 Field Device status	Contents of Un\G252
	D264	CH3 Field Device status	Contents of Un\G264

**Tab. 6-12:** List of used devices

**NOTE**

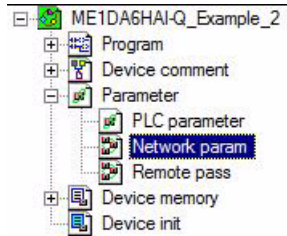
In this program example REMFR instructions are used to read the data from the buffer memory of the analog output module mounted to the remote I/O station. REMTO instructions are used to write data to the buffer memory of the analog output module. For further information about these instructions or the MELSECNET/H remote I/O network refer to the MELSECNET/H Network System Reference Manual.



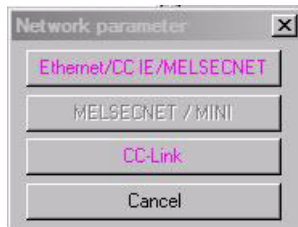
### 6.3.2 Network parameter

#### Network parameter setting

- Using the programming software, call up the **Network Parameter** selection box by double clicking on the highlighted option.



- When the box has been opened, select Ethernet/CCIE/MELSECNET.



This opens up the dialogue box to allow the MELSECNET module to be configured which can be seen below.

- In the **Network type** window, click on the down arrow, to show the available selections.

	Module 1	Module 2	M
Network type	None	None	None
Starting I/O No.			
Network No.			
Total stations			
Group No.			
Station No.			
Mode			

- ④ Select **MNET/H (Remote-Master)** and enter the other items as shown below.

	Module 1	Module 2
Network type	MNET/H(Remote master)	None
Starting I/O No.	0000	
Network No.	1	
Total stations	1	
Group No.		
Station No.		
Mode	On line	
	Network range assignment	
	Refresh parameters	
	Interrupt settings	

The dialogue box now shows the specific setting options for the module. The buttons in the bottom half of the table that are in red are for setting the mandatory parts of the module, those in magenta are optional.

- ⑤ Click on **Network range assignment** and **Switch screens** to **XY setting**.

**Network parameters Assignment the MNET/10(H) remote station network range. Module No.:**

Setup common parameters and I/O assignments.

Assignment method  
 Points/Start  
 Start/End

Monitoring time: 200 X 10ms  
 Total slave stations: 1  
 Parameter name:   
 Switch screens: XY setting

StationNo.	M station -> R station						M station			
	Y			Y			X			
	Points	Start	End	Points	Start	End	Points	Start	End	
1										

- ⑥ Enter the following:

Start/End  
 Total slave stations: 1  
 Switch screens: XY setting

StationNo.	M station -> R station						M station <- R station					
	Y			Y			X			X		
	Points	Start	End	Points	Start	End	Points	Start	End	Points	Start	End
1	256	0100	01FF	256	0000	00FF	256	0100	01FF	256	0000	00FF

- ⑦ **Switch screens** to **BW setting** and enter the following:

Start/End  
 Total slave stations: 1  
 Switch screens: BW setting

StationNo.	M station -> R station			M station <- R station			M station -> R station			M station <- R station		
	B			B			W			W		
	Points	Start	End	Points	Start	End	Points	Start	End	Points	Start	End
1							256	0000	00FF	256	0100	01FF

- ⑧ When the settings have been made, click **End** to return to the main network parameter setting window. Note that the **Network range assignment** button has now changed to blue, indicating that changes have been made.

	Module 1	Module 2
Network type	MNET/H(Remote master)	None
Starting I/O No.	0000	
Network No.	1	
Total stations	1	
Group No.		
Station No.		
Mode	On line	
	Network range assignment	
	Refresh parameters	
	Interrupt settings	

- ⑨ Next, click on **Refresh parameters** to bring up the following dialogue. This is where the settings for the data exchange between MELSECNET/H and PLC CPU will be made. Enter the values shown below.

	Link side					PLC side			
	Dev. name	Points	Start	End		Dev. name	Points	Start	End
Transfer SB	SB	512	0000	01FF	↔	SB	512	0000	01FF
Transfer S/W	S/W	512	0000	01FF	↔	S/W	512	0000	01FF
Random cyclic	LB				↔				
Random cyclic	LW				↔				
Transfer1	LB	8192	0000	1FFF	↔	B	8192	0000	1FFF
Transfer2	LW	8192	0000	1FFF	↔	W	8192	0000	1FFF
Transfer3	LX	512	0000	01FF	↔	X	512	0000	01FF
Transfer4	LY	512	0000	01FF	↔	Y	512	0000	01FF
Transfer5					↔				
Transfer6					↔				

- ⑩ When the settings have been made, click **End** to return to the main network parameter setting window.
- ⑪ Click **End** to check and close the main network parameter setting dialogue. These settings will be sent to the PLC next time the parameters are downloaded.

### 6.3.3 Program

- Remote I/O station status check

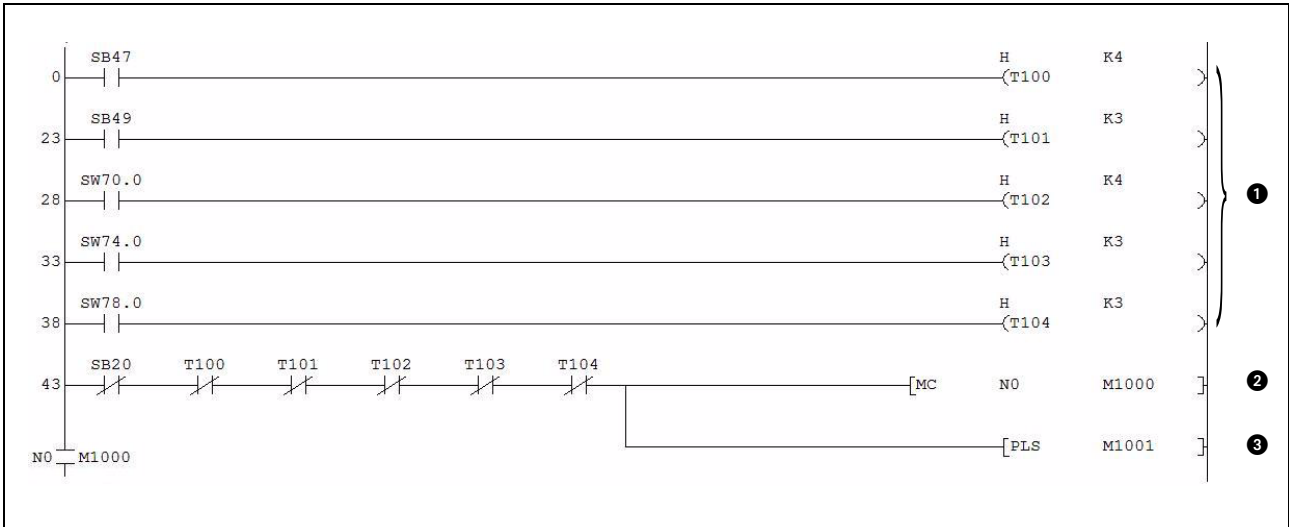


Fig. 6-17: Status checking of the remote I/O station

Number	Description
①	To prevent the control from stopping even if the network detects an instantaneous error due to a cable problem, noise or any other condition, the errors are delayed. Note that the above "4" and "3" represent standard values.
②	When the communication with the MELSECNET/H remote I/O station is without fault, the master control instruction is switched ON.
③	When the communication with the MELSECNET/H remote I/O station is possible, the initial setting request (M1001) is set.

Tab. 6-13: Description of the program shown above

**NOTE**

The following program for initial setting and processing of the ME1DA6HAI-Q will only be executed if the input condition of the master control instruction is set, i.e. M1000 is "1".

● Initial settings

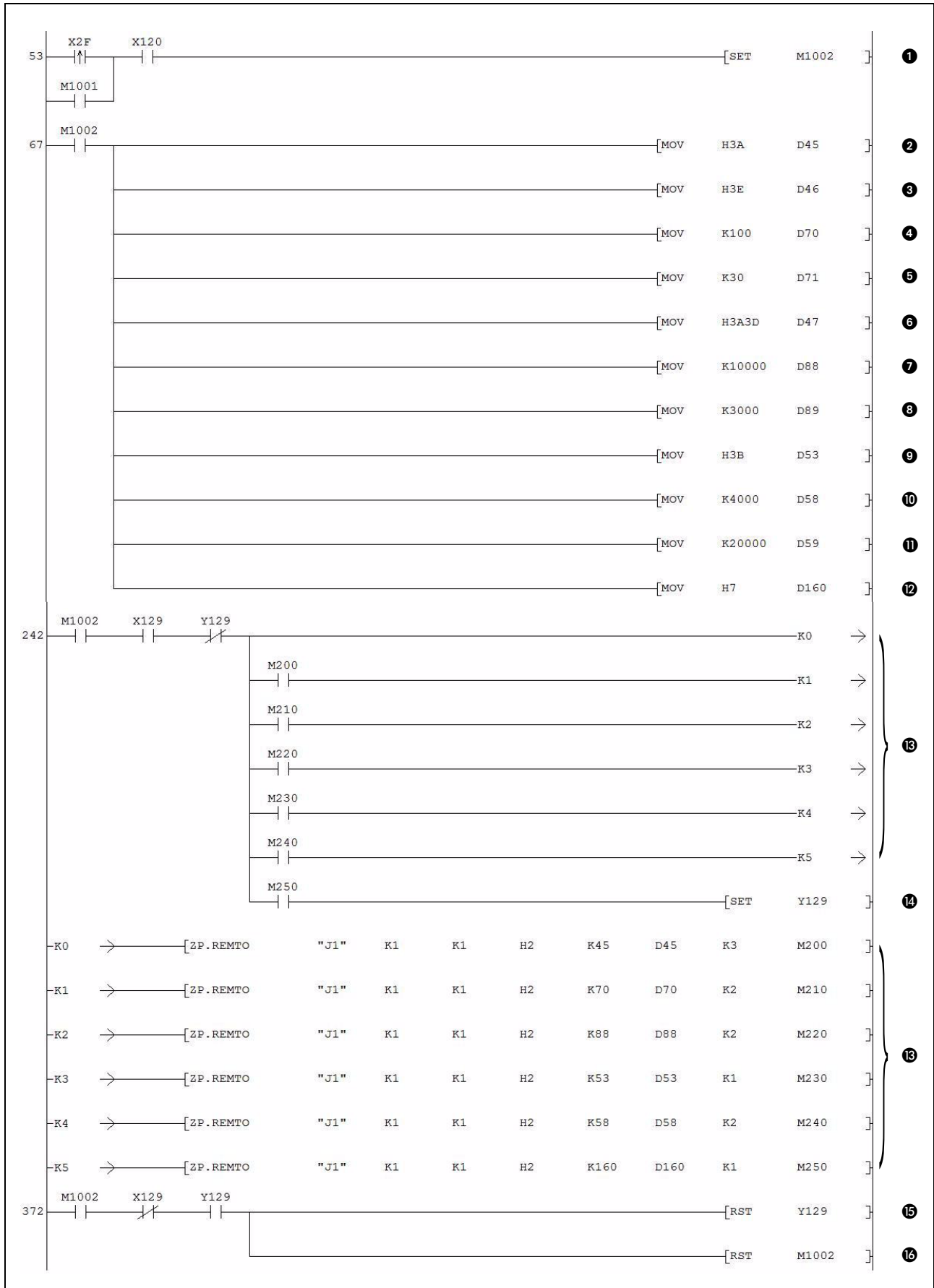


Fig. 6-18: Initial settings performed by the sequence program

Number	Description
①	When an initial setting command (X2F) or a request for initial setting of the ME1DA6HAI-Q (M1001) is issued, the internal relay M1002 ("Perform initial setting") is set
②	Short circuit detection enable/disable setting (CH1, CH3: enable)
③	Rate control enable/disable setting (CH1: enable)
④	Rate control: Setting of the CH1 increase digital limit value
⑤	Rate control: Setting of the CH1 decrease digital limit value
⑥	The following settings are written to the register D47 (Buffer memory address U0\G47): <ul style="list-style-type: none"> <li>High byte: Disconnection detection enable/disable setting (CH1, CH3: enable)</li> <li>Low byte: Warning output enable/disable setting (CH2: enable)</li> </ul>
⑦	CH2 warning output setting: Upper limit value
⑧	CH2 warning output setting: Lower limit value
⑨	Scaling enable/disable setting (CH3: enable)
⑩	Setting of the CH3 scaling lower limit value
⑪	Setting of the CH3 scaling upper limit value
⑫	HART enable/disable setting (CH1, CH2, CH3: HART enabled) These instructions are optional. If the HART devices are set and monitored with the tool MX CommDTM-HART, these instructions can be omitted.
⑬	The parameters are written to the buffer memory of the ME1DA6HAI-Q. Several REMTO instructions are used since these parameters are not consecutively in the buffer memory. They are executed successively because these REMTO instructions use all the same communication channel.
⑭	When the last REMTO instruction has been executed, the operation condition setting request is turned ON.
⑮	When the setting is completed, the operation condition setting request is turned OFF.
⑯	Since the initial setting is completed, the "Perform initial setting" relay is also reset.

Tab. 6-14: Description of the program shown above

● Communication with HART devices

The following part of the program is optional. If the HART devices are set and monitored with the tool MX CommDTM-HART, these instructions can be omitted. The HART enable/disable setting was done earlier in the initial settings (refer to ⑫ in fig. 5-18).

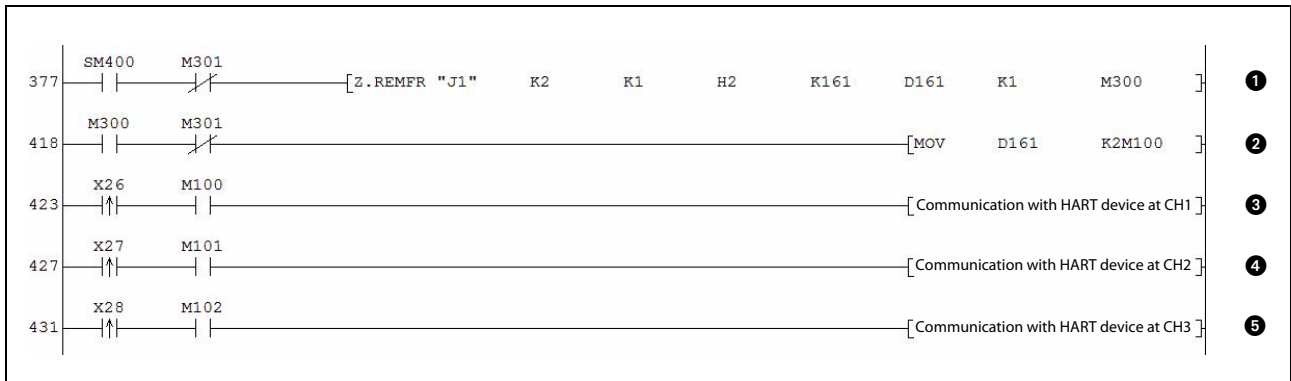


Fig. 6-19: Communication with HART devices

Number	Description	
①	The HART scan list is moved to the register D161. Since SM400 is always ON, this REMFR instruction is executed in every program cycle.	
②	When the REMFR instruction has been executed without an error, the HART scan list is moved to the internal relays M100 to M107.	
③	Sending of commands to the HART device, reading of information received from the HART device etc.	CH1
④		CH2
⑤		CH3

Tab. 6-15: Description of the program shown above

● Writing of digital values and analog output enable setting

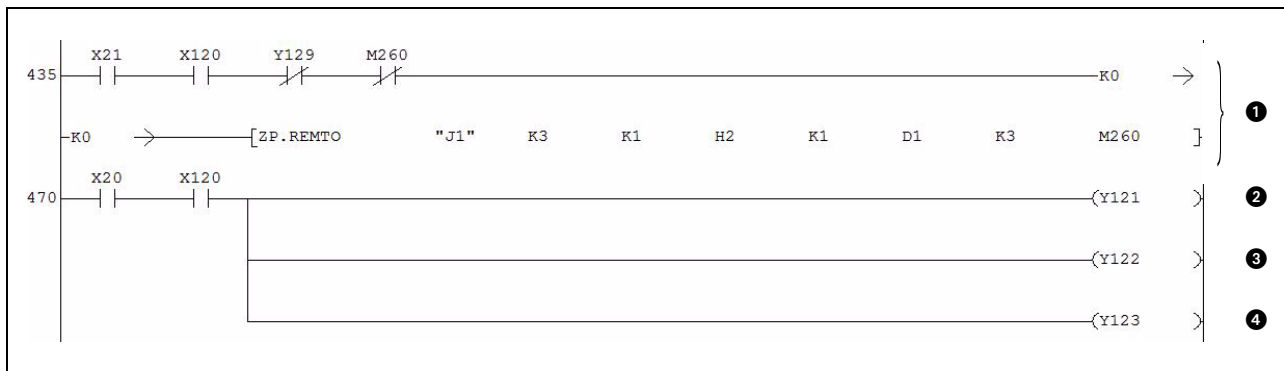


Fig. 6-20: Writing of the digital values to the ME1DA6HAI-Q

Number	Description	
1	The digital values are moved from the registers D1 to D3 where they were temporary stored by instructions elsewhere in the program to the buffer memory addresses Un\G1 to Un\G3.	
2	The analog output is enabled.	CH1
3		CH2
4		CH3

Tab. 6-16: Description of the program shown above

● Warning occurrence status and processing at warning occurrence

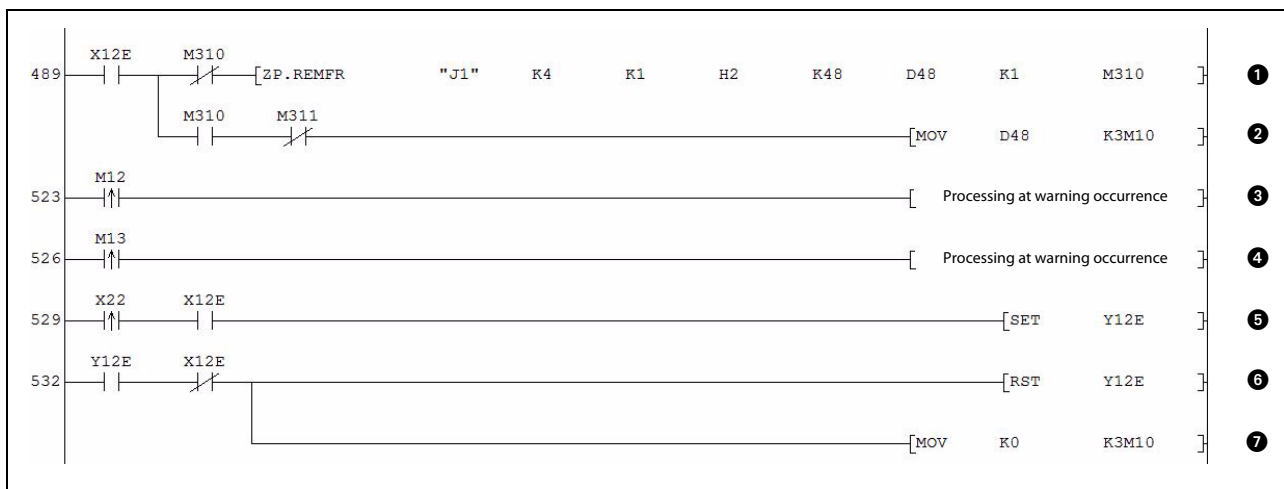


Fig. 6-21: Program part for warning processing

Number	Description	
1	When the warning output signal (X12E) is ON, the status of the warning output flags is moved to the register D48.	
2	When the REMFR instruction has been executed without an error, the status of the warning output flags is moved from D48 to the internal relays M10 to M21.	
3	Processing at warning occurrence	CH2 upper limit value warning
4		CH2 lower limit value warning
5	When X22 (Warning output reset signal) is switched ON while the warning output signal is ON, the warning output clear request (Y12E) is turned ON.	
6	When there is no warning indicated, the warning output clear request (Y12E) is turned OFF.	
7	The internal relays storing the warning output flags are also cleared.	

Tab. 6-17: Description of the program shown above

● Disconnection detection status and processing at disconnection detection

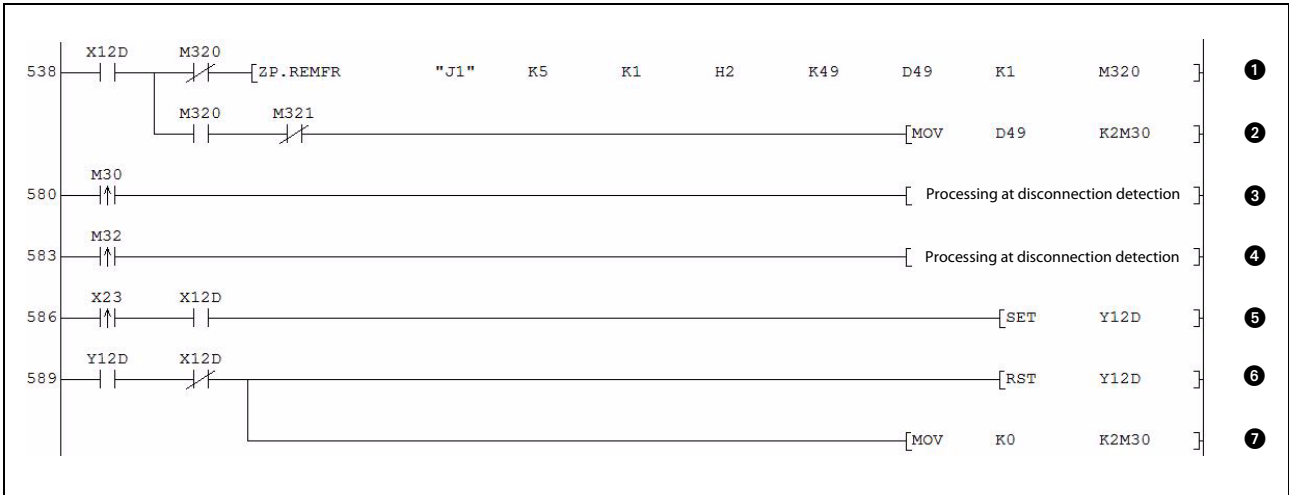


Fig. 6-22: Sequence program for disconnection detection

Number	Description	
①	When the disconnection detection signal (X12D) is ON, the status of the disconnection detection flags is moved to the register D49.	
②	When the REMFR instruction has been executed without an error the status of the disconnection detection flags is moved further to the internal relays M30 to M35	
③	Processing at disconnection detection	CH1
④		CH3
⑤	When X23 (Disconnection detection reset signal) is switched ON while the disconnection detection signal is ON, the disconnection detection clear request (Y12D) is turned ON.	
⑥	When there is no disconnection indicated, the disconnection detection clear request (Y12D) is turned OFF.	
⑦	The internal relays storing the disconnection detection flags are also cleared.	

Tab. 6-18: Description of the program shown above



● Short circuit detection status and processing at short circuit detection

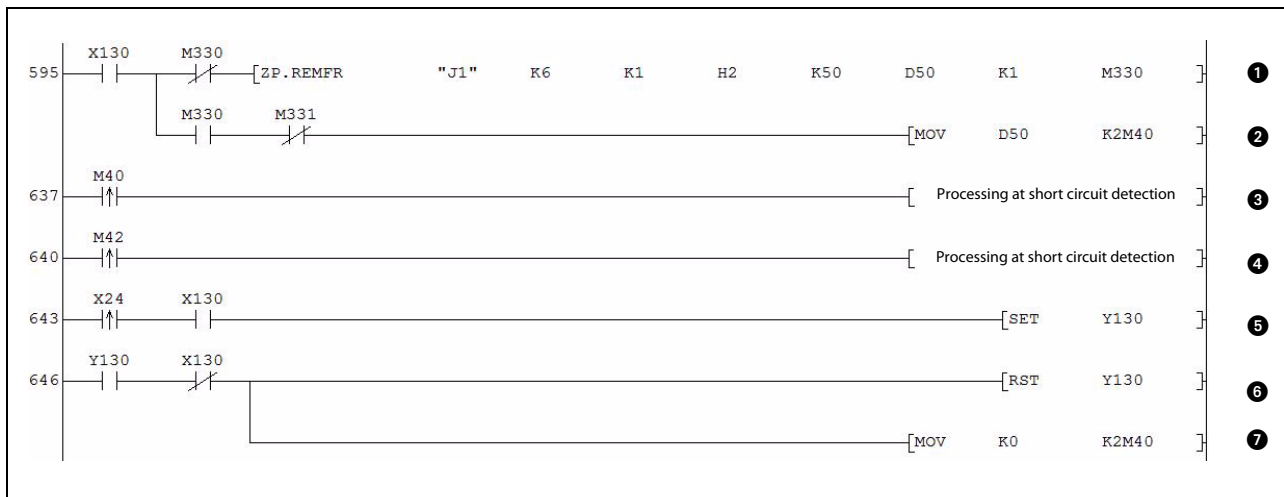


Fig. 6-23: Sequence program for short circuit detection

Number	Description	
①	When the short circuit detection signal (X130) is ON, the status of the short circuit detection flags is moved to the register D50.	
②	When the REMFR instruction has been executed without an error the status of the short circuit detection flags is moved to the internal relays M40 to M45.	
③	Processing at short circuit detection	CH1
④		CH3
⑤	When X24 (Short circuit detection reset signal) is switched ON while the short circuit detection signal is ON, the short circuit detection clear request (Y130) is turned ON.	
⑥	When there is no short circuit indicated, the short circuit detection clear request (Y130) is turned OFF.	
⑦	The internal relays storing the short circuit detection flags are also cleared.	

Tab. 6-19: Description of the program shown above

● Error detection and display

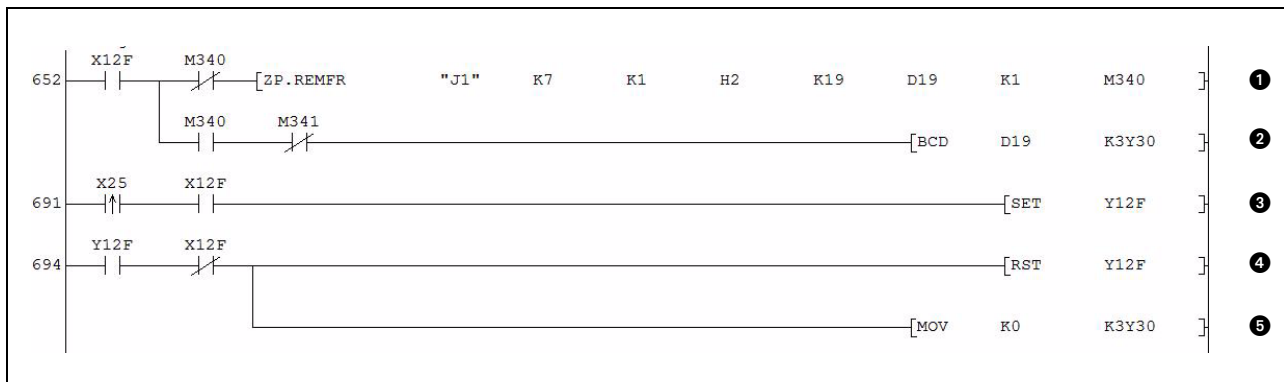


Fig. 6-24: Error detection, display and handling

Number	Description
①	In case of an error the error code the error code is read and stored in register D19.
②	When the REMFR instruction has been executed without an error the error code is output in BCD.
③	When an error has been detected and the reset signal (X25) is ON, the error clear request (Y12F) is set.
④	When there is no error indicated, the error clear request (Y12F) is turned OFF.
⑤	The error code outputs are also cleared.

Tab. 6-20: Description of the error detection and handling

● HART field device status check and processing at device malfunction

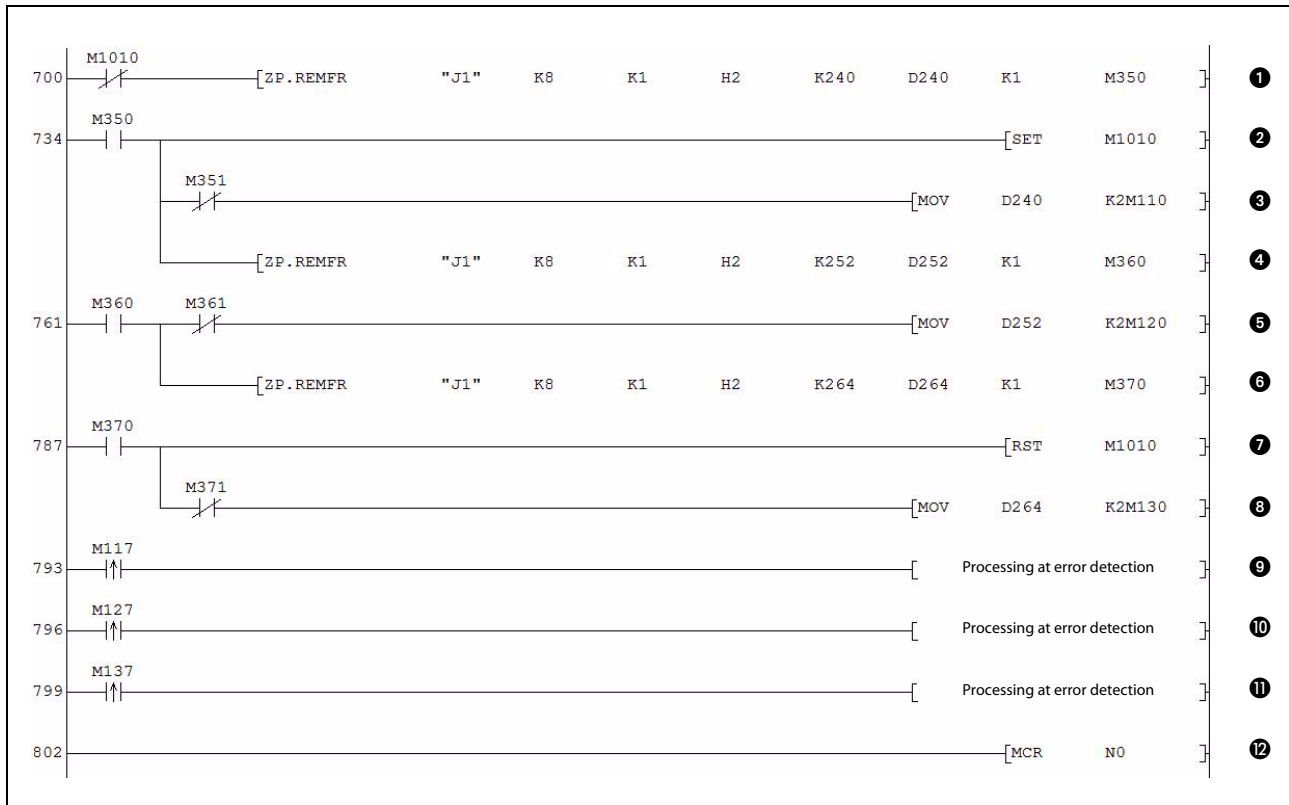


Fig. 6-25: HART field device status check and error processing

Number	Description	
①	The status of the device connected to CH1 is read and stored in D240.	
②	When the REMFR instruction has been executed an internal relay for controlling the scan sequence is set.	
③	When the REMFR instruction has been executed without an error the CH1 HART field device status is moved into M110 to M117.	
④	The next REMFR instruction, which reads the status of device connected to CH2, is started.	
⑤	When the REMFR instruction has been executed without an error the CH2 HART field device status is moved into M120 to M127.	
⑥	The next REMFR instruction, which reads the status of device connected to CH3, is started.	
⑦	After execution of the third REMFR instruction the internal relay controlling the execution sequence of the REMFR instructions is reset. In the next program scan the REMFR instruction for reading the CH1 field device status will be executed again.	
⑧	When the REMFR instruction has been executed without an error the CH2 HART field device status is moved into M130 to M137.	
⑨	Processing when a malfunction of a HART field device is detected.	Device malfunction at CH1
⑩		Device malfunction at CH2
⑪		Device malfunction at CH3
⑫	Master control reset (Only when the input condition for the MC instruction (fig. 5-18) is set, the instructions between the MC and the MCR instruction are executed.)	

Tab. 6-21: Description of the error detection and handling

# 7 Troubleshooting

The following section explains the types of errors that may occur when the HART analog output module ME1DA6HAI-Q is used, and how to troubleshoot such errors.

## 7.1 Error Code List

If an error occurs in the analog output module while writing to or reading data from the programmable controller CPU, an error code is written to buffer memory address 19 (Un\G19).

Error code (decimal)	Error description	Corrective action
10□	The output range is set with an illegal value in the intelligent function module switch setting in the PLC parameter. □ indicates the number of the channel set incorrectly.	Set a correct parameter value in the parameter setting using GX Developer or GX IEC Developer. (Refer to section 4.5.)
111	Hardware error of the module.	Turn the power OFF and ON again. If the error occurs again, the module may be malfunctioning. Please consult your local Mitsubishi representative, explaining the detailed description of the problem.
13□*1	HART communication error. The device answer is erroneous or timed out. □ indicates the channel number.	<ul style="list-style-type: none"> <li>Make sure the HART device's polling address is set to "0".</li> <li>Check the connection to the HART device.</li> <li>Increase the "HART Maximum Retries" setting in the buffer memory. (Refer to section 3.5.24.)</li> </ul>
60□*1	The specified digital value is outside the valid range. □ indicates the number of the channel set incorrectly.	Set a value that is within the valid range.
61□*1	The warning output upper/lower limit value setting is outside the range -32768 to 32767. □ indicates the number of the channel set incorrectly.	Correct the contents of the warning output upper limit value/lower limit value (Un\G86 to Un\G97) to within the range -32768 to 32767.
62□*1	The warning output lower limit value is equal to or greater than the warning output upper limit value. □ indicates the channel number.	Make setting so that the warning output lower limit value is lesser than the warning output upper limit value.
80□*1	The increase/decrease digital limit value setting is outside the range 0 to 32000. □ indicates the number of the channel set incorrectly.	Correct the contents of the buffer memory addresses Un\G70 to Un\G81 to within the range 0 to 32000.
90□*1	The scaling upper/lower limit value (Un\G54 to Un\G65) is set outside the range of -32768 to 32767. □ indicates the number of the channel set incorrectly.	Correct the scaling upper/lower limit value within the range of -32768 to 32767.
91□*1	In the scaling upper/lower limit value setting (Un\G54 to Un\G65) the lower limit is greater than the upper limit. □ indicates the number of the channel set incorrectly.	Set them again so that the scaling lower limit value is lesser than the scaling upper limit value.

**Tab. 7-1:** Error code list

### NOTES

When two or more errors have occurred, the latest error found by the analog output module is stored.

An error described with \*1 can be cleared by turning ON the error clear request (YF).

## 7.2 Troubleshooting using the LEDs of the Module

### 7.2.1 When the "RUN" LED is flashing or turned off

Check item	Corrective action
Is the intelligent function module setting switch 4 set to "other than 0"?	Using GX Developer or GX IEC Developer parameter setting, set the intelligent function module setting switch 4 to "0" (Refer to section 4.5).

**Tab. 7-2:** When the "RUN" LED is flashing

Check item	Corrective action
Is the power being supplied?	Confirm that the supply voltage for the power supply module is within the rated range.
Is the capacity of the power supply module adequate?	Calculate the current consumption of the CPU module, I/O modules and intelligent function modules mounted on the base unit to see if the power supply capacity is adequate.
Has a watchdog timer error occurred?	Reset the programmable controller CPU and verify that it is lit. If the RUN LED does not light even after doing this, the module may be malfunctioning. Please consult your local Mitsubishi representative, explaining the detailed description of the problem.
Is the module correctly mounted on the base unit?	Check the mounting condition of the module.

**Tab. 7-3:** When the "RUN" LED is off

### 7.2.2 When the "ERR." LED is on

Check item	Corrective action
Is an error being generated?	Confirm the error code and take corrective action described in section 6.1.

**Tab. 7-4:** When the "ERR" LED is on

### 7.2.3 When the "ALM" LED is on or flashing

Check item	Corrective action
Has a short circuit occurred?	Check the short circuit detection flag (buffer memory address Un\G50).

**Tab. 7-5:** When the "ALM" LED is on

Check item	Corrective action
Has disconnection occurred?	Check the disconnection detection flag (buffer memory address Un\G49).

**Tab. 7-6:** When the "ALM" LED is flashing

## 7.3 When an Analog Output Value is Not Output

Check item	Corrective action
Is 24 V DC external supply power being supplied?	Check that the external supply power terminals (terminals 15 (+24 V DC) and 16 (0V)) are supplied with a 24 V DC voltage.
Is there any fault with the analog signal lines such as disconnection or wire break?	Check for faulty condition of the signal lines by a visual check and a continuity check.
Is the CPU module in the STOP status?	Set the CPU module to the RUN status.
Is the output range setting correct?	Check the contents of the buffer memory addresses Un\G20 and Un\G21 in the monitor of GX Developer or GX IEC Developer. If the output range setting is incorrect, redo the GX (IEC) Developer intelligent function module switch setting (Refer to section 4.5).
Is the digital value being written to the channel to be output?	Verify the contents of the buffer memory addresses 1 to 6 (Un\G1 to Un\G6) in the monitor of GX Developer or GX IEC Developer.
Has the operating condition setting request (Y9) been executed?	From GX Developer or GX IEC Developer, turn the operating condition setting request (Y9) from ON to OFF and check that the analog output is normal. If normal analog output is obtained, review the initial setting of the sequence program (Refer to section 3.4.)

**Tab. 7-7:** Troubleshooting when an analog output value is not output

### NOTE

If the analog output value is not output after the proper corrective action is taken in accordance with the above check item, the possible cause is a module failure.  
Please consult your local Mitsubishi representative, explaining the detailed description of the problem.

## 7.4 When an Analog Output Value is Not Held

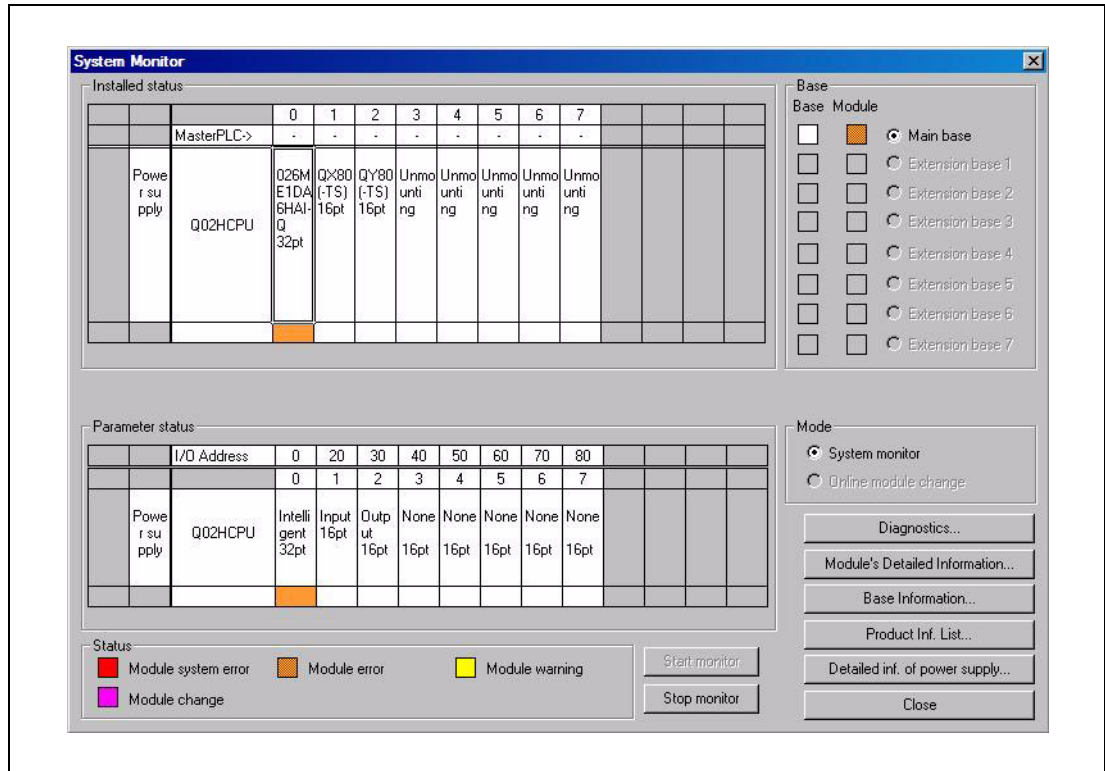
Check item	Corrective action
Is the HOLD/CLEAR setting correct?	Using GX Developer or GX IEC Developer parameter setting, check the setting of the intelligent function module setting switch 3 (Refer to section 4.5).
Is the D/A module used on a MELSECNET/H remote I/O station?	Please refer to the NOTE in section 3.3.1 and take corrective action.

**Tab. 7-8:** Troubleshooting when an analog value is not held while the CPU is placed in STOP or in a stop error status.

## 7.5 Checking the Analog Output Module Status

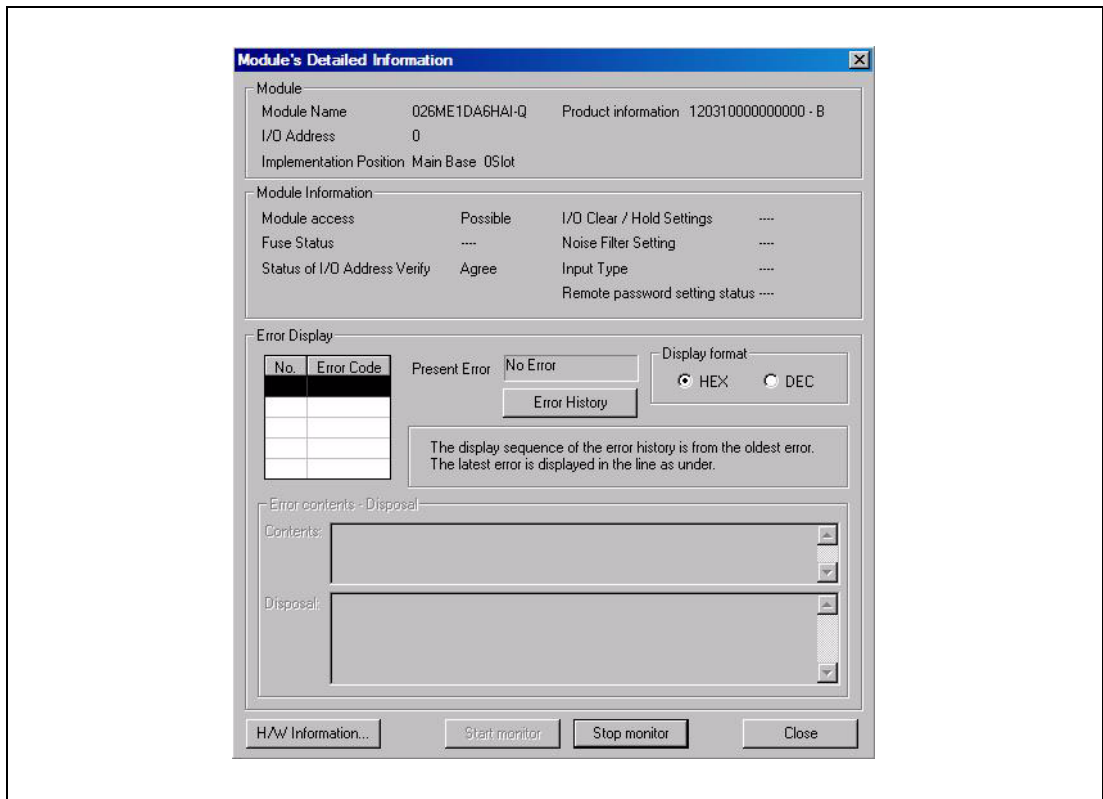
When the analog output module detail information is selected in GX Developer or GX IEC Developer system monitor, an error code and the status of the intelligent function module switch setting can be checked.

- Operating GX Developer  
In the **Diagnostics** menu select **System monitor**.
- Operating GX IEC Developer  
In the **Debug** menu select **System monitor**.



**Fig. 7-1:** The System Monitor displays comprehensive information of the connected PLC

For further information about a module, click on the module and then click **Module Detailed Information**.



**Fig. 7-2:** Detailed information on the selected module allow an easy and quick troubleshooting

**Contents of Module’s Detailed Information**

- Module
  - Module Name: Shows the designation of the module, e.g. ME1DA6HAI-Q
  - I/O Address: Head address of the module
  - Implementation Position: Shows whether the module is mounted to the main base or to an extension base and the position of the module.
  - Product information: Serial No. of the module. The letter shows the function version.
- Module Information
  - Module access: Shows whether the module is ready or not.
  - Fuse status: Not relevant for the HART analog output module ME1DA6HAI-Q.
  - Status of I/O Address Verify: Indicates whether the parameter set module and the installed module are identical.
  - I/O Clear / Hold Settings, Noise Filter Setting, etc.: Not relevant for the ME1DA6HAI-Q.
- Error Display
  - Checking the error code  
 The error code stored in buffer memory address 19 (Un\G19) of the ME1DA6HAI-Q is displayed in the **Present Error** field.  
  
 When the **Error History** button is pressed, the contents displayed in the **Present Error** field is displayed in the No. 1 field.





# Index

<b>A</b>		Error clear request (output signal) . . . . .	3-19
Accuracy . . . . .	3-5	Error code list . . . . .	7-1
ALM LED . . . . .	7-2	Error flag (input signal) . . . . .	3-18
Analog output HOLD/CLEAR function		External power supply	
Overview . . . . .	3-6	Specifications . . . . .	3-3
Settings with intelligent function module		Wiring . . . . .	4-5
switches . . . . .	4-7		
Troubleshooting . . . . .	7-3	<b>F</b>	
Analog output range		Function version . . . . .	2-3
I/O conversion characteristics . . . . .	3-4	<b>G</b>	
Settings with intelligent function module		GX Works2	
switches . . . . .	4-7	Auto refresh . . . . .	5-7
Auto refresh . . . . .	5-7	New intelligent function module . . . . .	5-1
<b>B</b>		Parameter setting for intelligent	
Buffer memory		function modules . . . . .	5-5
Overview . . . . .	3-21	Setting switches for intelligent	
Structure . . . . .	3-20	function modules . . . . .	5-3
<b>C</b>		<b>H</b>	
CHn output enable/disable flag (output signal) . .	3-19	HART	
Conversion time . . . . .	3-3	Command request . . . . .	3-44
Current output characteristics . . . . .	3-4	Date . . . . .	3-50
<b>D</b>		Descriptor . . . . .	3-47
D/A conversion		Device Function Flags . . . . .	3-49
Setting range . . . . .	3-33	Device ID . . . . .	3-48
Disconnection detection (input signal) . . . . .	3-17	Device Profile . . . . .	3-49
Disconnection detection clear request		Device Type . . . . .	3-48
(output signal) . . . . .	3-19	Final Assembly Number . . . . .	3-50
Disconnection detection function		Long Tag . . . . .	3-49
Enable/disable . . . . .	3-35	Manufacturer ID . . . . .	3-47
Flags in buffer memory . . . . .	3-36	Message . . . . .	3-47
Overview . . . . .	3-12	Private Label Distributor . . . . .	3-49
Program example (1) . . . . .	6-10	PV Damping Value . . . . .	3-51
Program example (2) . . . . .	6-24	PV Range Unit Code . . . . .	3-50
<b>E</b>		PV Upper and Lower Range Value . . . . .	3-51
Enable/disable setting		Revisions . . . . .	3-48
Disconnection detection . . . . .	3-35	Tag . . . . .	3-47
HART communication . . . . .	3-38	Transfer Function . . . . .	3-51
Rate control . . . . .	3-34	Unit Code . . . . .	3-51
Scaling function . . . . .	3-37	Write Protect . . . . .	3-50
Short circuit detection . . . . .	3-34		
Warning output function . . . . .	3-35		
ERR. LED . . . . .	7-2		

## HART Command

Answer Channel	3-46
Answer Code	3-46
Answer Data	3-46
Answer Data Size	3-46
Answer Flag	3-46
Request Channel	3-45
Request Code	3-45
Request Data	3-45
Request Data Size	3-45
Request Flag	3-44

## HART function

Applicable cables	4-5
Command answer	3-46
Communication enable/disable setting	3-38
Device variable status	3-42
Extended field device status	3-41
Field device status	3-40
Information about HART devices	3-47
Scan list	3-38
Write data error code	3-33

## HART Master function

	3-14
--	------

## HOLD/CLEAR function

Overview	3-6
Settings with intelligent function module switches	4-7

**I**

## Input signal

Disconnection detection	3-17
Error flag	3-18
Module ready	3-17
Operating condition setting completed	3-17
Short circuit detection signal	3-18
Warning output	3-17

## Intelligent function module parameter setting

	4-6
--	-----

## Intelligent function module switches

setting in GX Works2	5-3
setting in PLC parameters	4-7

**L**

## LEDs

ALM	7-2
ERR.	7-2
Overview	3-1
RUN	7-2

**M**

## ME1DA6HAI-Q

Accuracy	3-5
Dimensions	3-5
I/O assignment	4-6
I/O characteristics	3-4
Installation	4-3
Intelligent function module switch settings	4-7
LEDs	3-1
Parameter setting	4-6
Specifications	3-3

## MELSEC System Q CPU modules

	2-1
--	-----

## MELSECNET/H remote I/O station

	2-2
--	-----

## Module ready (input signal)

	3-17
--	------

## Multiple CPU system

	2-2
--	-----

## MX CommDTM-HART

	4-9
--	-----

**O**

## Online module change

	2-2
--	-----

## Operating condition

Setting completed flag	3-17
Setting request (output signal)	3-19

## Output range see Analog output range

## Output signal

CHn output enable/disable flag	3-19
Disconnection detection clear request	3-19
Error clear request	3-19
Operating condition setting request	3-19
Short circuit detection clear request	3-19
Warning output clear request	3-19

**R**

## Rate control function

Enable/disable setting	3-34
Increase/decrease digital limit values	3-37
Overview	3-8

## RUN LED

	7-2
--	-----

<b>S</b>		<b>T</b>	
Scaling function		Troubleshooting	7-2
Enable/disable settings	3-37		
Overview	3-10		
Upper/lower limit storage area	3-37		
Setting range	3-33		
Short circuit detection (input signal)	3-18		
Short circuit detection clear request (output signal)	3-19		
Short circuit detection function			
Enable/disable	3-34		
Flags in buffer memory	3-36		
Overview	3-13		
Program example (1)	6-11		
Program example (2)	6-25		
Switch settings for intelligent function module	4-7		
System monitor	7-4		
		<b>W</b>	
		Warning output (input signal)	3-17
		Warning output clear request (output signal)	3-19
		Warning output function	
		Enable/disable	3-35
		Flags in buffer memory	3-35
		Overview	3-11
		Program example (1)	6-10
		Program example (2)	6-23
		Upper/lower limit values.	3-38
		Wiring	
		Connection of external devices	4-5
		External power supply	4-5





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