S7-400H Instruction List

CPU 412-5H PN/DP, 414-5H PN/DP, 416-5H PN/DP, 417-5H PN/DP

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

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Contents

Applicability

This list of instructions applies to the CPUs listed below.

Name	Order number
CPU 412-5H PN/DP	6ES7 412–5HK06–0AB0
CPU 414-5H PN/DP	6ES7 414–5HM06–0AB0
CPU 416-5H PN/DP	6ES7 416–5HS06–0AB0
CPU 417-5H PN/DP	6ES7 417–5HT06–0AB0

Address Identifier and Parameter Ranges

Addr. ID	Parameter Range				Description
	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H	
Q [1]	0.0 to 255.7	0.0 to 255.7	0.0 to 1023.7	0.0 to 1023.7	Output (in PIQ)
QB [1]	0 to 255	0 to 255	0 to 1023	0 to 1023	Output byte (in PIQ)
QW [1]	0 to 254	0 to 254	0 to 1022	0 to 1022	Output word (in PIQ)
QD [1]	0 to 252	0 to 252	0 to 1020	0 to 1020	Output double word (in PIQ)
DBX	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in DB
DB	1 to 6000	1 to 6000	1 to 16000	1 to 16000	Data block
DBB	0 to 65533	0 to 65533	0 to 65533	0 to 65533	Data byte in DB
DBW	0 to 65532	0 to 65532	0 to 65532	0 to 65532	Data word in DB
DBD	0 to 65530	0 to 65530	0 to 65530	0 to 65530	Data double word in DB
DIX	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	0.0 to 65533.7	Data bit in instance DB
DI	1 to 6000	1 to 6000	1 to 16000	1 to 16000	Instance data block
DIB	0 to 65533	0 to 65533	0 to 65533	0 to 65533	Data byte in instance DB
DIW	0 to 65532	0 to 65532	0 to 65532	0 to 65532	Data word in instance DB
DID	0 to 65530	0 to 65530	0 to 65530	0 to 65530	Data double word in instance DB

[1] Default setting can be changed, see Technical Specifications

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range				Description
	CPU 412-5H	CPU 414-5H	CPU 414-5H	CPU 417-5H	
I [1)]	0.0 to 255.7	0.0 to 255.7	0.0 to 1023.7	0.0 to 1023.7	Input (in PII)
IB [1)]	0 to 255	0 to 255	0 to 1023	0 to 1023	Input byte (in PII)
IW [1)]	0 to 254	0 to 254	0 to 1022	0 to 1022	Input word (in PII)
ID [1)]	0 to 252	0 to 252	0 to 1020	0 to 1020	Input double word (in PII)
L [1)]	0.0 to 8191.7	0.0 to 8191.7	0.0 to 32767.7	0.0 to 32767.7	Local data
LB [1)]	0 to 8191	0 to 8191	0 to 32767	0 to 32767	Local data byte
LW [1)]	0 to 8191	0 to 8190	0 to 32766	0 to 32766	Local data word
LD [1)]	0 to 8191	0 to 8188	0 to 32764	0 to 32764	Local data double word
M	0.0 to 8191.7	0.0 to 8191.7	0.0 to 16383.7	0.0 to 16383.7	Bit memory
MB	0 to 8191	0 to 8191	0 to 16383	0 to 16383	Bit memory byte
MW	0 to 8190	0 to 8190	0 to 16382	0 to 16382	Bit memory word
MD	0 to 8188	0 to 8188	0 to 16380	0 to 16380	Bit memory double word

[1)] Default setting can be changed, see Technical Specifications

Address Identifier and Parameter Ranges, continued

Addr. ID	Parameter Range				Description
	CPU 412-5H	CPU 414-5H	CPU 414-5H	CPU 417-5H	
PQB	0 to 8191	0 to 8191	0 to 16383	0 to 16383	Peripheral output byte (direct I/O access)
PQW	0 to 8190	0 to 8190	0 to 16382	0 to 16382	Peripheral output word (direct I/O access)
PQD	0 to 8188	0 to 8188	0 to 16380	0 to 16380	Peripheral output double word (direct I/O access)
PIB	0 to 8191	0 to 8191	0 to 16383	0 to 16383	Peripheral input byte (direct I/O access)
PIW	0 to 8190	0 to 8190	0 to 16382	0 to 16382	Peripheral input word (direct I/O access)
PID	0 to 8188	0 to 8188	0 to 16380	0 to 16380	Peripheral input double word (direct I/O access)
T	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Timer
C	0 to 2047	0 to 2047	0 to 2047	0 to 2047	Counter

Constants and Ranges

Constant	Range	Description
B(b1,b2) B(b1,b2,b3,b4)	-	Constant, 2 or 4 bytes
D# Date	-	IEC date constant
L# Integer	-	32-bit integer constant
P# Bit pointer	-	Pointer constant
S5T# Time value	-	S7 time constant [1)]
T# TIme value	-	Time constant
TOD# Time value	-	IEC time constant
C# Count value	-	Counter constant (BCD code)
2#n	-	Binary constant
B#16# W#16# DW#16#	-	Hexadecimal constant

1) For loading of S7 timers

Abbreviations

The following abbreviations and mnemonics are used in the Instruction List:

Abbrev.	Description	Example
k8	8-bit constant 0 to 255	32
k16	16-bit constant 256 to 32 767	28 131
k32	32-bit constant 32 768 to 4 294 967 295	127 624
i8	8-bit integer -128 to +127	-113
i16	16-bit integer -32768 to +32767	+6523
i32	32-bit integer -2 147 483 648 to +2 147 483 647	-2 222 222
m	Pointer constant	P#240.3
n	Binary constant	1001 1100
p	Hexadecimal constant	EA12
Label	Symbolic jump address (max. 4 characters)	DESTINATION
a	Byte address	

Abbreviations, continued

Abbrev.	Description	Example
b	Bit address	
c	Address area	I, Q, M, L, DBX, DIX
d	Address in: MD, DBD, DID or LD	
e	Number in: MW, DBW, DIW or LW	
f	Timer/counter No.	
g	Address area	IB, QB, PIB, PQB, MB, LB, DBB, DIB
h	Address area	IW, QW, PIW, PQW, MW, LW, DBW, DIW
i	Address area	ID, QD, PID, PQD, MD, LD, DBD, DID
q	Block No.	

Registers

ACCU1 to ACCU4 (32 Bit)

The accumulators are registers for processing bytes, words or double words. The address identifiers are loaded into the accumulators, where they are logically gated. The result of the logic Instr. (RLO) is in ACCU1 and can be transferred from there to a memory cell.

The accumulators are 32 bits long.

Accumulator designations**:**

ACCU	Bit
ACCUx (x = 1 to 4)	Bit 0 to 31
ACCUx-L	Bit 0 to 15
ACCUx-H	Bit 16 to 31
ACCUx-LL	Bit 0 to 7
ACCUx-LH	Bit 8 to 15
ACCUx-HL	Bit 16 to 23
ACCUx-HH	Bit 24 to 31

Adress Registers AR1 and AR2 (32 Bit)

The address registers contain the area-internal or area-crossing pointers for instructions using indirect addressing. The address registers are 32 bits long. Die The area-internal and/or area-crossing pointers have the following syntax:

- Area-internal pointer: `00000000 00000bbb bbbbbbbb bbbbbxxx`
- Area-crossing pointer: **`yyyyyyyy`** `00000bbb bbbbbbbb bbbbbxxx`

Legend:

`b`	Byte address
`x`	Bit number
`y`	Area identifier (see “Examples of Addressing”)

Status word (16 Bits)

The status word bits are evaluated or set by the instructions.

The status word is 16 bits long.

Bit	Assignment	Description
0	/FC	First check bit
1	RLO	Result of logic Instr.
2	STA	Status
3	OR	Or (AND before OR)
4	OS	Stored overflow
5	OV	Overflow
6	CC 0	Condition code 0
7	CC 1	Condition code 1
8	BR	Binary result
9 to 15	Unassigned	-

Examples of Addressing

Addressing Examples	Description
Immediate Addressing	
L +27	Load 16-bit integer constant “27” into ACCU1
L L#-1	Load 32-bit integer constant “-1” into ACCU1
L 2#1010101010101010	Load binary constant into ACCU1
L DW#16#A0F0BCFD	Load hexadecimal constant into ACCU1
L ’ENDE’	Load ASCII character into ACCU1
L T#500 ms	Load time value into ACCU1
L C#100	Load count value into ACCU1
L B#(100,12)	Load 2-byte constant
L B#(100,12,50,8)	Load 4-byte constant
L P#10.0	Load area-internal pointer into ACCU1
L P#E20.6	Load area-crossing pointer into ACCU1
L -2.5	Load real number into ACCU1
L D# 1995-01-20	Load date
L TOD 13:20:33.125	Load time of day
Direct Addressing	
A I 0.0	ANDing of input bit 0.0
L IB 1	Load input byte 1 into ACCU1
L IW 0	Load input word 0 into ACCU1
L ID 0	Load input double word 0 into ACCU1

Examples of Addressing, continued

Addressing Examples	**Description**
Indirect Addressing of Timers/Counters	
SP T [LW 8]	Start timer; the timer number is in local data word 8
CU C [LW 10]	Count upwards; the counter number is in local data word 10
Area-Internal Memory-Indirect Addressing	
A I [LD 12] Example: L P#22.2 T LD 12 A I [LD 12]	AND Instr.: The address of the input is in local data double word 12 as pointer
A I [DBD 1]	AND Instr.: The address of the input is in data double word 1 of the open DB as pointer
A I [DID 12]	AND Instr.: The address of the output is in data double word 12 of the open instance DB as pointer
A I [MD 12]	AND Instr.: The address of the output is in memory double word 12 as pointer
Area-Internal Register-Indirect Addressing	
A I [AR1,P#12.2]	AND Instr.: The address of the input is calculated from the “pointer value in AR 1 $^{+}$ P#12.2”

Examples of Addressing, continued

Addressing Examples		**Description**	
Area-Internal Register-Indirect Addressing			
Area identifier	**Coding (binary)**	**hex.**	**Area**
P	1000 0**000**	80	I/O area
I	1000 0**001**	81	Input area
Q	1000 0**010**	82	Output area
M	1000 0**011**	83	Bit memory area
DB	1000 0**100**	84	Data area
DI	1000 0**101**	85	Instance data area
L	1000 0**110**	86	Local data area
VL	1000 0**111**	87	Predecessor local data area (access to local data of invoking block)
L B [AR1,P#8.0]		Load byte into ACCU1: The address is calculated from the “pointer value in AR 1 $^{+}$ P#8.0”	
A [AR1,P#32.3]		AND Instr.: The address of the operand is calculated from the “pointer value in AR 1 $^{+}$ P#32.3”	
Addressing Via Parameters			
A Parameter		Addressing via parameters	

Examples of how to calculate the pointer

- **Example for sum of bit addresses ≤ 7:**
  LAR1 P#8.2
  U E [AR1,P#10.2]
  Result: Input 18.4 is addressed (by adding the byte and bit addresses)
- **Example for sum of bit addresses >7:**
  L P#10.5
  LAR1
  U E [AR1,P#10.7]
  Result: Input 21.4 is addressed (by adding the byte and bit addresses with carry over)

Execution Times with Indirect Addressing

When using indirect addresses statement consists of two parts:

Part 1: Load the address of the instruction

Part 2: Execute the instruction

In other words, when working with indirect addresses, you must calculate the execution time of an instruction from these two parts.

Calculating the Execution Time

The total execution time is calculated as follows:

Time required for loading the address
\+ execution time of the instruction
= Total execution time of the instruction

The execution times listed in the chapter entitled “List of Instructions” apply to the execution times of the second part of an instruction, i.e. for the actual execution of an instruction.

You must then add the time required for loading the address of the instruction to this execution time (see following Table).

The execution time for loading the address of the instruction from the various areas is shown in the following table.

Addresse is in ...	**Execution Time in ns**			
	CPU 412-5H	**CPU 414-5H**	**CPU 416-5H**	**CPU 417-5H**
Bit memory area M				
Word	62.55	37.5	25	15
Double word	62.55	37.5	25	15
Data block DB/DX				
Word	78.19	46.88	31.31	18.75
Double word	78.19	46.88	31.31	18.75
Local data area L				
Word	62.55	37.5	25	15
Double word	62.55	37.5	25	15
AR1/AR2 (area-internal)	0.0 [1)]	0.0 [1)]	0.0 [1)]	0.0 [1)]
AR1/AR2 (area-crossing)	0.0 [1)]	0.0 [1)]	0.0 [1)]	0.0 [1)]
Parameter (word) ... for:				
• Timers	78.19	46.88	31.31	18.75
• Counters	78.19	46.88	31.31	18.75
• Block calls	78.19	46.88	31.31	18.75
Parameter (double word) ... for				
Bits, bytes, words and double words	78.19	46.88	31.31	18.75

1 Address registers AR1/AR2 do not need to be loaded in separate cycles for addressing

Examples of Calculations

You will find a few examples here for calculating the execution times for the various methods of indirect addressing.

Calculating the Execution Times for Area-Internal Memory-Indirect Addressing

Example: A I [DBD 12] with CPU 414

Step 1: Load the contents of DBD 12 (time required is listed in the table on page 20)

Address is in ...	Execution Time in ns
Bit memory area M	
Word	18.75
Double word	18.75
Data block DB/DX	46.88
Double word	

Step 2: AND the input addressed in this way (execution time see page 4)

Typical Execution Time in ns	
Direct Addressing	**indirecte Adressing**
18.75	Time for IE 46.88+

Total execution time

46.88 ns

\+ 18.75 ns

65.63 ns

- **Execution Time for Area-Crossing Register-Indirect Addressing**

  Example: U [AR1, P#23.1] ... with I 1.0 in AR1 with CPU 416

  1. Step: Load the contents of AR1, and increment them by the offset 23.1 (the time required is in the table on page 19)

Address is in ...	Execution Time in ns
:	:
AR1/AR2 (Area-crossing)	
:	:

  2. Step: AND link of the input addressed this way (see page 24 for the execution time 24)

Execution Time in ns	
Direct Addressing	**Indirect Addressing**
13.25 :	Time for AI 0+

Total execution time

```
        0 ns
+   13.25 ns
    13.25 ns
```

List of Instructions

This chapter contains the complete list of instructions for the S7-400H CPUs. The descriptions have been kept as concise as possible. You will find a detailed functional description in the various STEP 7 reference manuals.

Please note that, in the case of indirect addressing (examples see page 16), you must add the time required for loading the address of the particular instruction to the execution times listed (see page 19).

Bit Logic Instructions

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RLO from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the /FC bit is set to zero

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
U/UN		AND/AND-NOT					
	I/Q a.b	Input/output	1 [2] /2	31.28	18.75	13.2	7.5
	M a.b	Bit memory	1 [3] /2	31.28	18.75	13.2	7.5
	L a.b	Local data bit	2	31.28	18.75	13.2	7.5
	DBX a.b	Data bit	2	46.91	28.13	18.79	11.25
	DIX a.b	Instance data bit	2	46.91	28.13	18.79	11.25
	c [d]	Memory-indirect, area-internal [1]	2	31.28+/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	c [AR1,m]	Register-ind., area-internal (AR1) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	c [AR2,m]	Register-ind., area-internal (AR2) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	[AR1,m]	Area-crossing (AR1) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	[AR2,m]	Area-crossing (AR2) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	Parameter	Via parameter [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +

1 I, Q, M, L / DB, DI
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Bit Logic Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
O/ON		OR/OR-NOT					
	I/Q a.b	Input/output	1 [2]/2	31.28	18.75	13.2	7.5
	M a.b	Bit memory	1 [3]/2	31.28	18.75	13.2	7.5
	L a.b	Local data bit	2	31.28	18.75	13.2	7.5
	DBX a.b	Data bit	2	46.91	28.13	18.79	11.25
	DIX a.b	Instance data bit	2	46.91	28.13	18.79	11.25
	c [d]	Memory-indirect, area-internal [1]	2	31.28+/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	c [AR1,m]	Register-ind., area-internal (AR1) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	c [AR2,m]	Register-ind., area-internal (AR2) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	[AR1,m]	Area-crossing (AR1) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	[AR2,m]	Area-crossing (AR2) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	Parameter	Via parameter [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +

Status word for: **O, ON**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

[1] I, Q, M, L / DB, DI
[2] With direct instruction addressing; Address area 0 to 127
[3] With direct instruction addressing; Address area 0 to 255
\+ Plus time required for loading the address of the instruction (see page 20)

Bit Logic Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
X/XN		EXKLUSIV-OR/ EXKLUSIV-OR-NOT					
	E/A a.b	Input/output	2	31.28	18.75	13.2	7.5
	M a.b	Bit memory	2	31.28	18.75	13.2	7.5
	L a.b	Local data bit	2	31.28	18.75	13.2	7.5
	DBX a.b	Data bit	2	46.91	28.13	18.79	11.25
	DIX a.b	Instance data bit	2	46.91	28.13	18.79	11.25
	c [d]	Memory-indirect, area-internal. [1]	2	31.28+/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	c [AR1,m]	Register-ind., area-internal (AR1) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	c [AR2,m]	Register-ind., area-internal (AR2) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	[AR1,m]	Area-crossing (AR1) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	[AR2,m]	Area-crossing (AR2) [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +
	Parameter	Via parameter [1]	2	31.28 +/46.91 +	18.75 +/28.13 +	13.2 +/18.79 +	7.5 + /11.25 +

Status word for: **X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

[1] I, Q, M, L / DB, DI

\+ Plus time required for loading the address of the instruction (see page 20)

Bit Logic Instructions with Parenthetical Expressions

Saving the RLO and OR bits and the relevant function identifier (A, AN, ...) to the nesting stack. Seven nesting levels are possible per block. After the right parenthesis, the logic operation indicated by the function identifier is performed on the saved RLO and the current RLO; the current OR is overwritten with the saved OR.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
A(		AND left parenthesis	1	31.28	18.75	13.2	7.5
AN(		AND NOT left parenthesis	1	31.28	18.75	13.2	7.5
O(		OR left parenthesis	1	31.28	18.75	13.2	7.5
ON(		OR NOT left parenthesis	1	31.28	18.75	13.2	7.5
X(		EXCLUSIVE OR left parenthesis	1	31.28	18.75	13.2	7.5
XN(		EXCLUSIVE OR NOT left parenthesis	1	31.28	18.75	13.2	7.5

Status word for: **A(, AN(, O(, ON(, X(, XN(**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	1	-	0

Bit Logic Instructions with Parenthetical Expressions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
)		Right parenthesis, removing an entry from the nesting stack.	1	31.28	18.75	13.2	7.5

Status word for:)	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	Yes	1	Yes	1

ORing of AND Instructions

The ORing of AND instructions is implemented according to the rule: AND before OR

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
O		ORing of AND operations according to the rule: AND before OR	1	31.28	18.75	13.2	7.5

Status word for: **O**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	1	-	Yes

Logic Instructions with Timers and Counters

Examining the status of the addressed timer/counter and gating the result with the RLO according to the appropriate logic function.

Instr.	Address ID	Description	Length in words	Execution Time ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
A/AN		AND/AND NOT					
	T f	Timer	1[1]/2	31.28	18.75	13.2	7.5
	T [e]	Timer, memory-indirect addressing	2	31.28+	18.75+	13.2+	7.5+
	Z f	Counter	1[1]/2	31.28	18.75	13.2	7.5
	Z [e]	Counter, memory-indirect addressing	2	31.28+	18.75+	13.2+	7.5+
	Timer para. Counter para.	Timer/counter (addressing via parameter)	2	31.28+ 31.28+	18.75+ 18.75+	13.2+ 13.2+	7.5+ 7.5+

Status word for: **A, AN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

[1] With direct instruction addressing; Address area 0 to 255
\+ Plus time required for loading the address of the instruction (see page 20)

Logic Instructions with Timers and Counters, continued

Instr.	Address ID	Description	Length in words	Execution Time ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
O/ON		OR/OR-NOT					
	T f	Timer	1[1])/2	31.28	18.75	13.2	7.5
	T [e]	Timer, memory-indirect addr.	2	31.28+	18.75+	13.2+	7.5+
	Z f	Counter	1[1])/2	31.28	18.75	13.2	7.5
	Z [e]	Counter, memory-indirect addressing	2	31.28+	18.75+	13.2+	7.5+
	Timerpara. Zählerpara.	Timer/counter (addressing via parameter)	2	31.28+ 31.28+	18.75+ 18.75+	13.2 13.2	7.5 7.5
X/XN		EXCLUSIVE OR/EXCLUSIVE OR NOT					
	T f	Timer	2	31.28	18.75	13.2	7.5
	T [e]	Timer, memory-indirect addr.	2	31.28+	18.75+	13.2+	7.5+
	Z f	Counter	2	31.28	18.75	13.2	7.5
	Z [e]	Counter, mem.-indirect addr.	2	31.28+	18.75+	13.2+	7.5+
	Timer para. Counter para.	EXCLUSIVE OR timer/counter (addressing via parameter)	2	31.28+ 31.28+	18.75+ 18.75+	13.2+ 13.2+	7.5+ 7.5+

Status word for: **O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	Yes
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

1) With direct instruction addressing; Address area 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Word Logic Instructions with the Contents of Accumulator 1

Gating the contents of ACCU1 and/or ACCU1-L with a word or double word according to the appropriate function. The word or double word is either specified in the instruction as an address or is in ACCU2. The result is in ACCU1 and/or ACCU1-L.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
AW		AND ACCU2-L	1	31.28	18.75	13.2	7.5
AW	W#16#p	AND 16-bit constant	2	31.28	18.75	13.2	7.5
OW		OR ACCU2-L	1	31.28	18.75	13.2	7.5
OW	W#16#p	OR 16-bit constant	2	31.28	18.75	13.2	7.5
XOW		EXCLUSIVE OR ACCU2-L	1	31.28	18.75	13.2	7.5
XOW	W#16#p	EXCLUSIVE-OR 16-bit constant	2	31.28	18.75	13.2	7.5

Status word for: **AW, OW, XOW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

Word Logic Instructions with the Contents of Accumulator 1, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
AD		AND ACCU2	1	31.28	18.75	13.2	7.5
AD	DW#16#p	AND 32-bit constant	3	31.28	18.75	13.2	7.5
OD		OR ACCU2	1	31.28	18.75	13.2	7.5
OD	DW#16#p	OR 32-bit constant	3	31.28	18.75	13.2	7.5
XOD		EXCLUSIVE OR ACCU2	1	31.28	18.75	13.2	7.5
XOD	DW#16#p	EXCLUSIVE OR 32-bit constant	3	31.28	18.75	13.2	7.5

Status word for: **AD, OD, XOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

Evaluating Conditions Using AND, OR and EXCLUSIVE OR

All logic instructions generate a result (new RLO). The first instruction in a logic string generates the new RLO from the signal state scanned. The subsequent logic instructions generate the new RL from the signal state scanned and the old RLO. The logic string ends with an instruction which limits the RLO (e.g. a memory instruction); that is, the FC bit is set to zero.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
A/AN O/ON X/XN		AND/AND NOT OR/OR-NOT EXCLUSIVE OR/ EXCLUSIVE-OR-NOT					
	==0	Result=0 (CC1=0 and CC0=0)	1	31.28	18.75	13.2	7.5
	>0	Result>0 (CC1=1 and CC0=0)	1	31.28	18.75	13.2	7.5
	<0	Result<0 (CC1=0 and CC0=1)	1	31.28	18.75	13.2	7.5
	<>0	Result≠0 ((CC1=0 and CC0=1) or (CC1=1 and CC0=0))	1	31.28	18.75	13.2	7.5

Status word for: **A, AN, O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
A/AN O/ON X/XN	<=0	Result>=0 ((CC1=1 and CC0=0) or (CC1=0 and CC0=0))	1	31.28	18.75	13.2	7.5
	>=0	Result<=0 ((CC1=0 and CC0=1) or (CC1=0 and CC0=0))	1	31.28	18.75	13.2	7.5

Status word for: **A, AN, O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Evaluating Conditions Using AND, OR and EXCLUSIVE OR, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
A/AN O/ON X/XN		AND/AND-NOT OR/OR-NOT EXCLUSIVE-OR/ EXCLUSIVE-OR-NOT					
	UO	Unordered math instruction (CC1=1 and CC0=1)	1	31.28	18.75	13.2	7.5
	OS	AND OS=1	1	31.28	18.75	13.2	7.5
	BR	AND BR=1	1	31.28	18.75	13.2	7.5
	OV	AND OV=1	1	31.28	18.75	13.2	7.5

Status word for: **A, AN, O, ON, X, XN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	Yes	-	Yes	Yes
Instruction affects:	-	-	-	-	-	Yes	Yes	Yes	1

Edge-Triggered Instructions

The current RLO is compared with the status of the instruction or “edge bit memory”. FP detects a change from “0” to “1”; FN detects a change from “1” to “0”.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
FP/FN	I/Q a.b	The positive/negative edge is indicated by RLO = 1. The bit addressed in the instruction is the auxiliary edge bit memory.	2	31.28	18.75	13.2	7.5
	M a.b		2	31.28	18.75	13.2	7.5
	L a.b [1]		2	31.28	18.75	13.2	7.5
	DBX a.b		2	78.19	46.88	31.31	18.75
	DIX a.b		2	78.19	46.88	31.31	18.75
	c [d] [2]		2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	c [AR1,m] [2]		2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	c [AR2,m] [2]		2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	[AR1,m] [2]		2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	[AR2,m] [2]		2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	Parameter [2]		2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+

Status word for: **FP, FN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	Yes	Yes	1

1 Unnecessary if the bit being monitored is in the process image (local data of a block are only valid while the block is running).
2 I, Q, M, L /DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Setting/Resetting Bit Addresses

Assigning the value “1” or “0” to the addressed instruction when RLO = 1. The instructions can be dependent on the MCR (see page 4).

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
S		Set addressed bit to “1”					
R		Set addressed bit to “0”					
	I/Q a.b	Input/output	1[2]/2	31.28	18.75	13.2	7.5
	M a.b	Bit memory	1[3]/2	31.28	18.75	13.2	7.5
	L a.b	Local data bit	2	31.28	18.75	13.2	7.5
	DBX a.b	Data bit	2	78.19	46.88	31.31	18.75
	DIX a.b	Instance data bit	2	78.19	46.88	31.31	18.75
	c [d]	Memory-indirect, area-internal [1]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	c [AR1,m]	Register-ind., area-internal (AR1) [1]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	c [AR2,m]	Register-ind., area-internal (AR2) [1]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	[AR1,m]	Area-crossing (AR1) [1]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	[AR2,m]	Area-crossing (AR2) [1]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	Parameter	Via parameter [1]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+

Status word for: **S, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	Yes	-	0

1 I, Q, M, L / DB, DI
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
\+ Plus time required for loading the address of the instruction (see page 20)

Setting/Resetting Bit Addresses, continued

The RLO is written to the address of the instruction. The instructions can be dependent on the MCR (see page 93).

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
=		Assign RLO					
	I/Q a.b	to Input/output	1[2)]/2	31.28	18.75	13.2	7.5
	M a.b	to Bit memory	1[3)]/2	31.28	18.75	13.2	7.5
	L a.b	to Local data bit	2	31.28	18.75	13.2	7.5
	DBX a.b	to DData bit	2	78.19	46.88	31.31	18.75
	DIX a.b	to Instance data bit	2	78.19	46.88	31.31	18.75
	c [d]	Memory-indirect, area-internal [1)]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	c [AR1,m]	Register-ind., area-internal (AR1) [1)]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	c [AR2,m]	Register-ind., area-internal (AR2) [1)]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	[AR1,m]	Area-crossing (AR1) [1)]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	[AR2,m]	Area-crossing (AR2) [1)]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+
	Parameter	Via parameter [1)]	2	31.28+/78.19+	18.75+/46.88+	13.2+/31.31+	7.5+/18.75+

Status word for: =	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	Yes	-	0

1 I, Q, M, L / DB, DI
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Instructions Directly Affecting the RLO

The following instructions have a direct effect on the RLO.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
CLR		Set RLO to "0"	1	31.28	18.75	13.2	7.5

Status word for: **CLR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	0	0	0

SET		Set RLO to "1"	1	31.28	18.75	13.2	7.5

Status word for: **SET**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	1	1	0

NOT		Negate RLO	1	31.28	18.75	13.2	7.5

Status word for: **NOT**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	Yes	-	Yes	-
Instruction affects:	-	-	-	-	-	-	1	Yes	-

SAVE		Save RLO to the BR bit	1	31.28	18.75	13.2	7.5

Status word for: **SAVE**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	Yes	-	-	-	-	-	-	-	-

Timer Instructions

Starting or resetting a timer. The time value must be in ACCU1-L. The instructions are triggered by an edge transition in the RLO; that is, when the status of the RLO has changed between two calls.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
SP	T f T [e]	Start timer as pulse on edge change from “0” to “1”	1[1])/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timerpara.		2	78.19+	46.88+	31.31+	18.75+
SE	T f T [e]	Start timer as extended pulse on edge change from “0” to “1”	1[1])/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timerpara.		2	78.19+	46.88+	31.31+	18.75+
SD	T f T [e]	Start timer as ON delay on edge change from “0” to “1”	1[1])/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timer para.		2	78.19+	46.88+	31.31+	18.75+

Status word for: **SP, SE, SD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1 With direct instruction addressing; Address area 0 to 255
\+ Plus time required for loading the address of the instruction (see page 20)

Timer Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
SS	T f T [e]	Start timer as retentive ON delay on edge change from “0” to “1”	1[1)]/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timer para.		2	78.19+	46.88+	31.31+	18.75+
SF	T f T [e]	Start timer as OFF delay on edge change from “0” to “1”	1[1)]/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timer para.		2	78.19+	46.88+	31.31+	18.75+

Status word for: **SS, SF**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct instruction addressing; Address area 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Timer Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
FR	T f T [e]	Enable timer for restarting on edge change from “0” to “1” (reset edge bit memory for starting timer)	1[1)]/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timer para.		2	78.19+	46.88+	31.31+	18.75+
R	T f T [e]	Reset timer	1[1)]/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Timer para.		2	78.19+	46.88+	31.31+	18.75+

Status word for: **FR, R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct instruction addressing; Address area 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Counter Instructions

The count value must be in ACCU1-L in the form of a BCD number (0-999).

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
S	Z f Z [e]	Presetting of counter on edge change from “0” to “1”	1[1])/2	62.55 62.55+	37.5 37.5+	25.05 25.05+	15 15+
	Counter para.		2	62.55+	37.5+	25.05+	15+
R	Z f Z [e]	Reset counter to “0” when RLO = “1”	1[1])/2	62.55 62.55+	37.5 37.5+	25.05 25.05+	15 15+
	Counter para.		2	62.55+	37.5+	25.05+	15+
CU	Z f Z [e]	Increment counter by 1 on edge change from “0” to “1”	1[1])/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Counter para.		2	78.19+	46.88+	31.31+	18.75+

Status word for: **S, R, CU**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

[1]) With direct instruction addressing; Address area 0 to 255
\+ Plus time required for loading the address of the instruction (see page 20)

Counter Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
CD	Z f Z [e]	Decrement counter by 1 on edge change from “0” to “1”	1[1)]/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Counter para.		2	78.19+	46.88+	31.31+	18.75+
FR	Z f Z [e]	Enable counter on edge change from “0” to “1” (reset edge bit memory for up and down counting and setting the counter)	1[1)]/2	78.19 78.19+	46.88 46.88+	31.31 31.31+	18.75 18.75+
	Counter para.		2	78.19+	46.88+	31.31+	18.75+

Status word for: **CD, FR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	-	-	0

1) With direct instruction addressing; Address area 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Load Instructions

Loading address identifiers into ACCU1. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L		Load ...					
	EB a	Input byte	1[2]/2	31.28	18.75	13.2	7.5
	AB a	Output byte	1[2]/2	31.28	18.75	13.2	7.5
	PEB a	Peripheral input byte (solo [1])	1[2]/2	31.28	18.75	13.2	7.5
		Peripheral input byte (redundant)					
	MB a	Bit memorybyte	1[3]/2	31.28	18.75	13.2	7.5
	LB a	Local data byte	2	31.28	18.75	13.2	7.5
	DBB a	Data byte	2	31.28	18.75	13.2	7.5
	DIB a	Instance data byte	2	31.28	18.75	13.2	7.5
		... into ACCU1					
	g [d]	Memory-indirect, area-internal. [4]	2	31.28 +	18.75 +	13.2 +	7.5 +
	g [AR1,m]	Register-ind., area-internal (AR1) [4]	2	31.28 +	18.75 +	13.2 +	7.5 +
	g [AR2,m]	Register-ind., area-internal (AR2) [4]	2	31.28 +	18.75 +	13.2 +	7.5 +
	B[AR1,m]	Area-crossing (AR1) [4]	2	31.28 +	18.75 +	13.2 +	7.5 +
	B[AR2,m]	Area-crossing (AR2) [4]	2	31.28 +	18.75 +	13.2 +	7.5 +
	Parameter	Via parameter [4]	2	31.28 +	18.75 +	13.2 +	7.5 +

1 Plus acknowledgment time of the I/O module (> 1 µs), bus runtimes and synchronization time in redundant mode
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
4 I, Q, P, M, L / DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Load Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

Instr.	Address ID	Description	Length in words	Execution time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L		Load ...					
	IW a	Input word	1[2)]/2	31.28	18.75	13.2	7.5
	QW a	Output word	1[2)]/2	31.28	18.75	13.2	7.5
	PIW a	Peripheral input word (solo [1)])	1[2)]/2	31.28	18.75	13.2	7.5
		Peripheral input word (redundant)					
	MW a	Bit memory word	1[3)]/2	31.28	18.75	13.2	7.5
	LW a	Local data word	2	31.28	18.75	13.2	7.5
	DBW a	Data word	2	31.28	18.75	13.2	7.5
	DIW a	Instance data word	2	31.28	18.75	13.2	7.5
		... into ACCU1-L					
	h [d]	Memory-indirect, area-internal [4)]	2	31.28 +	18.75 +	13.2 +	7.5 +
	h [AR1,m]	Register-ind., area-internal (AR1) [4)]	2	31.28 +	18.75 +	13.2 +	7.5 +
	h [AR2,m]	Register-ind., area-internal (AR2) [4)]	2	31.28 +	18.75 +	13.2 +	7.5 +
	W[AR1,m]	Area-crossing (AR1) [4)]	2	31.28 +	18.75 +	13.2 +	7.5 +
	W[AR2,m]	Area-crossing (AR2) [4)]	2	31.28 +	18.75 +	13.2 +	7.5 +
	Parameter	Via parameter[4)]	2	31.28 +	18.75 +	13.2 +	7.5 +

1 Plus acknowledgment time of the I/O module (> 1 µs), bus runtimes and synchronization time in redundant mode
2) With indirect instruction addressing; Address area 0 to 127
3 With direct instruction addressing; Address area 0 to 255
4 I, Q, P, M, L / DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Load Instructions, continued

the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L		Load ...					
	ID a	Input double word	1[2)]/2	31.28	18.75	13.2	7.5
	QD a	Output double word	1[2)]/2	31.28	18.75	13.2	7.5
	PID a	Peripheral-Input double word (solo [1)])	2	31.28	18.75	13.2	7.5
		Peripheral-Input double word (redundant)					
	MD a	Bit memory double word	1[3)]/2	31.28	18.75	13.2	7.5
	LD a	Lokaldaten double word	2	31.28	18.75	13.2	7.5
	DBD a	Data double word	2	46.91	28.13	18.79	11.25
	DID a	Instance data double word	2	46.91	28.13	18.79	11.25
		... into ACCU1					
	i [d]	Memory-indirect, area-internal [4)]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	i [AR1,m]	Register-ind., area-internal (AR1) [4)]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	i [AR2,m]	Register-ind., area-internal (AR2) [4)]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	D[AR1,m]	Area-crossing (AR1) [4)]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	D[AR2,m]	Area-crossing (AR2) [4)]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	Parameter	Via parameter[4)]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+

1 Plus acknowledgment time of the I/O module (> 1 µs), bus runtimes and synchronization time in redundant mode
2) With indirect instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
4 I, Q, P, M, L / DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Load Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L		Load ...					
	k8	8-bit constant into ACCU1-LL	2	31.28	18.75	13.2	7.5
	k16	16-bit constant into ACCU1-L	2	31.28	18.75	13.2	7.5
	k32	32-bit constant into ACCU1	3	31.28	18.75	13.2	7.5
	Parameter	Load constant into ACCU1 (from parameter)	2	46.91+	28.13+	18.79	11.25+
L	2#n	Load 16-bit binary constant into ACCU1-L	2	31.28	18.75	13.2	7.5
		Load 32-bit binary constant into ACCU1	3	31.28	18.75	13.2	7.5
	B#16#p	Load 8-bit-hexadecimal constant into ACCU1-L	1	31.28	18.75	13.2	7.5
L	W#16#p	Load 16-bit hexadecimal constant into ACCU1-L	2	31.28	18.75	13.2	7.5
	DW#16#p	Load 32-bit hexadecimal constant into ACCU1	3	31.28	18.75	13.2	7.5

+ Plus time required for loading the address of the instruction (see page 20)

Load Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L	'x'	Load 1 character	2	31.28	18.75	13.2	7.5
	'xx'	Load 2 characters	2	31.28	18.75	13.2	7.5
	'xxx'	Load 3 characters	3	31.28	18.75	13.2	7.5
	'xxxx'	Load 4 characters	3	31.28	18.75	13.2	7.5
L	D# Zeitwert	Load IEC date	3	31.28	18.75	13.2	7.5
L	S5T# Zeitwert	Load S7 time constant (16 bits)	2	31.28	18.75	13.2	7.5
L	TOD# Zeitwert	Load IEC time constant	3	31.28	18.75	13.2	7.5
L	T# Zeitwert	Load 16-bit time constant	2	31.28	18.75	13.2	7.5
		Load 32-bit time constant	3	31.28	18.75	13.2	7.5
L	C# Zählwert	Load counter constant (BCD code)	2	31.28	18.75	13.2	7.5
L	B# (b1, b2)	Load constant as byte (b1, b2)	2	31.28	18.75	13.2	7.5
	B# (b1, b2, b3, b4)	Load constant as 4 bytes (b1, b2, b3, b4)	3	31.28	18.75	13.2	7.5

Load Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L	P# Bi tpointer	Load bit pointer	3	31.28	18.75	13.2	7.5
L	L# Integer number	Load 32-bit integer constant	3	31.28	18.75	13.2	7.5
L	Real number	Load floating-point number	3	31.28	18.75	13.2	7.5

Load Instructions for Timers and Counters

Loading a time value or count value into ACCU1. The contents of ACCU1 are first saved to ACCU2. The bits of the status word are not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L	T f T [e]	Load time value	1[1)]/2 2	31.28 31.28+	18.75 18.75+	13.2 13.2+	7.5 7.5+
	Timer para.	Load time value (addressed via parameter)	2	31.28+	18.75+	13.2+	7.5+
L	Z f Z [e]	Load count value	1[1)]/2 2	31.28 31.28+	18.75 18.75+	13.2 13.2+	7.5 7.5+
	Counter para.	Load count value (addressed via parameter)	2	31.28+	18.75+	13.2+	7.5+
LC	T f T [e]	Load time value in BCD	1[1)]/2 2	31.28 31.28+	18.75 18.75+	13.2 13.2+	7.5 7.5+
	Timer para.	Load time value in BCD (addressed via parameter)	2	31.28+	18.75+	13.2+	7.5+
LC	Z f Z [e]	Load count value in BCD	1[1)]/2 2	31.28 31.28+	18.75 18.75+	13.2 13.2+	7.5 7.5+
	Counter para.	Load count value in BCD (addressed via parameter)	2	31.28+	18.75+	13.2+	7.5+

1) With direct instruction addressing; timer/counter no. 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)

Transfer Instructions

Transferring the contents of ACCU1 to the addressed operand. Note that some instructions are affected by the MCR (see page 4). The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
T		Transfer contents of ACCU1-LL to ...					
	IB a	input byte	1[2]/2	31.28	18.75	13.2	7.5
	QB a	output byte	1[2]/2	31.28	18.75	13.2	7.5
	PQB	peripheral output byte [1]	1[2]/2	31.28	18.75	13.2	7.5
	MB a	bit memory byte	1[3]/2	31.28	18.75	13.2	7.5
	LB a	local data byte	2	31.28	18.75	13.2	7.5
	DBB a	data byte	2	46.91	28.13	18.79	11.25
	DIB a	instance data byte	2	46.91	28.13	18.79	11.25
	g [d]	Memory-indirect, area internal [4]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	g [AR1,m]	Register-ind., area-internal (AR1) [4]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	g [AR2,m]	Register-ind., area-internal (AR2) [4]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	B[AR1,m]	Area-crossing (AR1) [4]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	B[AR2,m]	Area-crossing (AR2) [4]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+
	Parameter	Via parameter [4]	2	31.28+/46.91+	18.75+/28.13+	13.2+/18.79+	7.5+/11.25+

1) Plus acknowledgment time of the I/O module (> 1 µs), bus runtimes and synchronization time in redundant mode
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
4 I, Q, P, M, L / DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Transfer Instructions, continued

If there is a remainder of 3 following an integral division of the used addresses by 4, the execution times for instructions specified on this page are doubled.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
T		Transfer contents of ACCU1-L to ...					
	IW a	Input word	1[2])/2	31.28	18.75	13.2	7.5
	QW a	Output word	1[2])/2	31.28	18.75	13.2	7.5
	PQW a	peripheral output word [1)]	1[2])/2	31.28	18.75	13.2	7.5
	MW a	Bit memory word	1[3])/2	31.28	18.75	13.2	7.5
	LW a	Local data word	2	31.28	18.75	13.2	7.5
	DBW a	Data word	2	93.82	56.26	37.58	22.5
	DIW a	Instance data word	2	93.82	56.26	37.58	22.5
	h [d]	Memory-indirect, area internal [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	h [AR1,m]	Register-ind., area-internal (AR1) [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	h [AR2,m]	Register-ind., area-internal (AR2) [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	W[AR1,m]	Area-crossing (AR1) [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	W[AR2,m]	Area-crossing (AR2) [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	Parameter	Via parameter [4)]	2	31.28+/93.82+	18.75+56.26+	13.2+/37.58+	7.5+/22.5+

1) Plus acknowledgment time of the I/O module (> 1 µs), bus runtimes and synchronization time in redundant mode
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
4 I, Q, P, M, L / DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Transfer Instructions, continued

If the used address is divisible by 4without a remainder, the execution times for instructions specified on this page is doubled.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
T		Transfer contents of ACCU1 to ...					
	ID a	Input double word	1[2)]/2	31.28	18.75	13.2	7.5
	QD a	Output double word	1[2)]/2	31.28	18.75	13.2	7.5
	PQD a	Periph. output double word [1)]	2	31.28	18.75	13.2	7.5
	MD a	Bit memory double word	1[3)]/2	31.28	18.75	13.2	7.5
	LD a	Local data double word	2	31.28	18.75	13.2	7.5
	DBD a	Data double word	2	93.82	56.26	37.58	22.5
	DID a	Instance data double word	2	93.82	56.26	37.58	22.5
T	i [d]	Memory-indirect, area internal [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	i [AR1,m]	Register-ind., area-internal (AR1)[4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	i [AR2,m]	Register-ind., area-internal (AR2) [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	D[AR1,m]	Area-crossing (AR1) [4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+
	D[AR2,m]	Area-crossing (AR2) [4)]	2	31.28+/93.82+	18.75+56.26+	13.2+/37.58+	7.5+/22.5+
	Parameter	Via parameter[4)]	2	31.28+/93.82+	18.75+/56.26+	13.2+/37.58+	7.5+/22.5+

1) Plus acknowledgment time of the I/O module (> 1 µs), bus runtimes and synchronization time in redundant mode
2) With direct instruction addressing; Address area 0 to 127
3) With direct instruction addressing; Address area 0 to 255
4 I, Q, P, M, L / DB, DI
\+ Plus time required for loading the address of the instruction (see page 20)

Load and Transfer Instructions for Address Registers

Loading a double word from a memory area or register into address register 1 (AR1) or address register 2 (AR2). The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
LAR1		Load contents from ...					
	-	ACCU1	1	31.28	18.75	13.2	7.5
	AR2	Address register 2	1	31.28	18.75	13.2	7.5
	DBD	Data double word	2	46.91	28.13	19.8	11.25
	DID a	Instance data double word	2	46.91	28.13	19.8	11.25
	m	32-bit constant as pointer	3	31.28	18.75	13.2	7.5
	LD a	Local data double word	2	31.28	18.75	13.2	7.5
	MD a	Bit memory double word	2	31.28	18.75	13.2	7.5
		... into AR1					
LAR2		Load contents from ...					
	-	ACCU1	1	31.28	18.75	13.2	7.5
	DBD a	Data double word	2	46.91	28.13	19.8	11.25
	DID a	Instance data double word	2	46.91	28.13	19.8	11.25
	m	32-bit constant as pointer	3	31.28	18.75	13.2	7.5
	LD a	Local data double word	2	31.28	18.75	13.2	7.5
	MD a	Bit memory double word	2	31.28	18.75	13.2	7.5
		... into AR2					

Load and Transfer Instructions for Address Registers, continued

Transferring a double word from address register 1 (AR1) or address register 2 (AR2) to a memory area or register. The contents of ACCU1 are first saved to ACCU2. The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
TAR1		Transfer contents from AR1 in ...					
	-	ACCU1	1	31.28	18.75	13.2	7.5
	AR2	Address register 2	1	31.28	18.75	13.2	7.5
	DBD a	Data double word	2	93.82	56.26	39.6	22.5
	DID a	Instance data double word	2	93.82	56.26	39.6	22.5
	LD a	Local data double word	2	31.28	18.75	13.2	7.5
	MD a	Bit memory double word	2	31.28	18.75	13.2	7.5
TAR2		Transfer contents from AR2 in ...					
	-	ACCU1	1	31.28	18.75	13.2	7.5
	DBD a	Data double word	2	93.82	56.26	39.6	22.5
	DID a	Instance data double word	2	93.82	56.26	39.6	22.5
	LD a	Local data double word	2	31.28	18.75	13.2	7.5
	MD a	Bit memory double word	2	31.28	18.75	13.2	7.5
CAR		Exchange the contents of AR1 and AR2	1	31.28	18.75	13.2	7.5

Load and Transfer Instructions for the Status Word

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L	STW	Load status word into ACCU1	1	31.28	18.75	13.2	7.5

Status word for: **L**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Instruction affects:	-	-	-	-	-	-	-	-	-

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
T	STW	Transfer ACCU1 (bits 0 to 8) to the status word	1	31.28	18.75	13.2	7.5

Status word for: **T**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Load Instructions for DB Number and DB Length

Loading the number/length of a data block into ACCU1. The old contents of ACCU1 are saved to ACCU2. The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
L	DBNO	Load number of data block	1	31.28	18.75	13.2	7.5
L	DINO	Load number of instance data block	1	31.28	18.75	13.2	7.5
L	DBLG	Load length of data block into byte	1	31.28	18.75	13.2	7.5
L	DILG	Load length of instance data block into byte	1	31.28	18.75	13.2	7.5

Integer Math (16 Bits)

Math instructions on two 16-bit words. The result is written to ACCU1 and/or ACCU1-L. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
+I		Add 2 integers (16 bits) (ACCU1-L)=(ACCU1-L)+(ACCU2-L)	1	31.28	18.75	13.2	7.5
-I		Subtract 2 integers (16 bits) (ACCU1-L)=(ACCU2-L)-(ACCU1-L)	1	31.28	18.75	13.2	7.5

Status word for: **+I, -I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Integer Math (16 Bits), continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
*I		Multiply 1 integer by another (16 bits) (ACCU1)=(ACCU2-L)*(ACCU1-L)	1	31.28	18.75	13.2	7.5
/I		Divide 1 integer by another (16 bits) (ACCU1-L)=(ACCU2-L):(ACCU1-L) The remainder is in ACCU1-H.	1	125.03	67	52.8	30

Status word for: ***I, /I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Integer Math (32 Bits)

Math instructions on two 32-bit words. The result is written to ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
+D		Add 2 integers (32-bit) (ACCU1)=(ACCU2)+(ACCU1)	1	31.28	18.75	13.2	7.5
-D		Subtract 2 integers (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	31.28	18.75	13.2	7.5
*D		Multiply 2 integers (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	31.28	18.75	13.2	7.5

Status word for: **+D, -D, *D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Integer Math (32 Bits), continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
/D		Divide 2 integers (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	187.65	112.5	75.15	45
MOD		Divide 2 integers (32 bits) and load the remainder into ACCU1: (ACCU1)=remainder of [(ACCU2):(ACCU1)]	1	187.65	112.5	75.15	45

Status word for: **/D, MOD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Floating-Point Math (32 Bits)

The result of the math instruction is in ACCU1. ACCU3 and ACCU4 are then transferred to ACCU2 and ACCU3.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
+R		Add 2 real numbers (32 bits) (ACCU1)=(ACCU2)+(ACCU1)	1	62.56	37.5	26.4	15
-R		Subtract 2 real numbers (32 bits) (ACCU1)=(ACCU2)-(ACCU1)	1	62.56	37.5	26.4	15
*R		Multiply 2 real numbers (32 bits) (ACCU1)=(ACCU2)*(ACCU1)	1	62.56	37.5	26.4	15
/R		Divide 2 real numbers (32 bits) (ACCU1)=(ACCU2):(ACCU1)	1	187.65	112.5	75.15	45

Status word for: **+R, -R, *R, /R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Floating-Point Math (32 Bits), continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
NEGR		Negate the real number in ACCU1	1	31.28	18.75	13.2	7.5
ABS		Form the absolute value of the real number in ACCU1	1	31.28	18.75	13.2	7.5

Status word for: **NEGR, ABS**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Square Root and Square Instructions (32 Bits)

The result of the instruction is in ACCU1. The SQRT instruction can be interrupted.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
SQRT		Calculate the square root of a real number in ACCU1	1	250.06	134	105.6	60
SQR		Form the square of the real number in ACCU1	1	62.56	37.5	26.4	15

Status word for: **SQRT, SQR**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Logarithmic Function (32 Bits)

The result of the logarithmic function is in ACCU1. The instructions can be interrupted.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
LN		Form the natural logarithm of a real number in ACCU1	1	656.78	393.75	263.03	157.5
EXP		Calculate the exponential value of a real number in ACCU1 to the base e (= 2.71828)	1	656.78	393.75	263.03	157.5

Status word for: **LN, EXP**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Trigonometrical Functions (32 Bits)

The result of the instruction is in ACCU1. The instructions can be interrupted.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
SIN		Calculate the sine of a real number	1	625.5	375	250.5	150
ASIN		Calculate the arcsine of a real number	1	2032.88	1218.75	814.13	487.5
COS		Calculate the cosine of a real number	1	625.5	375	250.5	150
ACOS		Calculate the arccosine of a real number	1	2064.15	1237.5	826.65	495
TAN		Calculate the tangent of a real number	1	844.43	506.25	338.18	202.5
ATAN		Calculate the arctangent of a real number	1	594.23	356.25	237.98	142.5

Status word for: **SIN, ASIN, COS, ACOS, TAN, ATAN**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Adding Constants

Adding integer constants and storing the result in ACCU1. The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
+	i8	Add an 8-bit integer constant	1	31.28	18.75	13.2	7.5
+	i16	Add a 16-bit integer constant	2	31.28	18.75	13.2	7.5
+	i32	Add a 32-bit integer constant	3	31.28	18.75	13.2	7.5

Adding Using Address Registers

Adding a 16-bit integer to the contents of the address register. The value is either specified as an address in the instruction or is in ACCU1-L. The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
+AR1		Add the contents of ACCU1-L to those of AR1	1	31.28	18.75	13.2	7.5
+AR1	m (0 to 4095)	Add a pointer constant to the contents of AR1	2	31.28	18.75	13.2	7.5
+AR2		Add the contents of ACCU1-L to those of AR2	1	31.28	18.75	13.2	7.5
+AR2	m (0 to 4095)	Add pointer constant to the contents of AR2	2	31.28	18.75	13.2	7.5

Comparison Instructions (16-Bit Integers)

Comparing the 16-bit integers in ACCU1-L and ACCU2-L. RLO = 1 if the condition is satisfied.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
==I		ACCU2-L=ACCU1-L	1	31.28	18.75	13.2	7.5
<>I		ACCU2-L≠ACCU1-L	1	31.28	18.75	13.2	7.5
<I		ACCU2-L<ACCU1-L	1	31.28	18.75	13.2	7.5
<=I		ACCU2-L<=ACCU1-L	1	31.28	18.75	13.2	7.5
>I		ACCU2-L>ACCU1-L	1	31.28	18.75	13.2	7.5
>=I		ACCU2-L>=ACCU1-L	1	31.28	18.75	13.2	7.5

Status word for: **==I, < >I, <I, <=I, >I, >=I**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	0	-	0	Yes	Yes	1

Comparison Instructions (32-Bit Integers)

Comparing the 32-bit integers in ACCU1 and ACCU2. RLO = 1 if the condition is satisfied.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
==D		ACCU2=ACCU1	1	31.28	18.75	13.2	7.5
<>D		ACCU2≠ACCU1	1	31.28	18.75	13.2	7.5
<D		ACCU2<ACCU1	1	31.28	18.75	13.2	7.5
<=D		ACCU2<=ACCU1	1	31.28	18.75	13.2	7.5
>D		ACCU2>ACCU1	1	31.28	18.75	13.2	7.5
>=D		ACCU2>=ACCU1	1	31.28	18.75	13.2	7.5

Status word for: **==D, < >D, <D, <=D, >D, >=D**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	0	-	0	Yes	Yes	1

Comparison Instructions (32-Bit Real Numbers)

Comparing the 32-bit real numbers in ACCU1 and ACCU2.
RLO = 1 if the condition is satisfied.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
==R		ACCU2=ACCU1	1	31.28	18.75	13.2	7.5
<>R		ACCU2≠ACCU1	1	31.28	18.75	13.2	7.5
<R		ACCU2<ACCU1	1	31.28	18.75	13.2	7.5
<=R		ACCU2<=ACCU1	1	31.28	18.75	13.2	7.5
>R		ACCU2>ACCU1	1	31.28	18.75	13.2	7.5
>=R		ACCU2>=ACCU1	1	31.28	18.75	13.2	7.5

Status word for: **==R, < >R, <R, <=R, >R, >=R**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	0	Yes	Yes	1

Shift Instructions

Shifting the contents of ACCU1 and ACCU1-L to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC 1.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
SLW [1]		Shift the contents of ACCU1-L to the left. Positions that become free are provided with zeros.	1	31.28	18.75	13.2	7.5
SLW	0 ... 15						
SLD		Shift the contents of ACCU1 to the left. Positions that become free are provided with zeros.	1	31.28	18.75	13.2	7.5
SLD	0 ... 32						
SRW [1]		Shift the contents of ACCU1-L to the right. Positions that become free are provided with zeros.	1	31.28	18.75	13.2	7.5
SRW	0 ... 15						

Status word for: **SLW, SLD, SRW**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

[1] No. of places shifted: 0 to 16

Shift Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
SRD		Shift the contents of ACCU1 to the right. Positions that become free are provided with zeros.	1	31.28	18.75	13.2	7.5
SRD	0 ... 32						
SSI [1]		Shift the contents of ACCU1-L with sign to the right. Positions that become free are provided with with the sign (bit 15).	1	31.28	18.75	13.2	7.5
SSI	0 ... 15						
SSD		Shift the contents of ACCU1 with sign to the right. Positions that become free are provided with with the sign (bit 31).	1	31.28	18.75	13.2	7.5
SSD	0 ... 32						

Status word for: **SRD, SSI, SSD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

[1] No. of places shifted: 0 to 16

Rotate Instructions

Rotate the contents of ACCU1 to the left or right by the specified number of places. If no address identifier is specified, the contents of ACCU2-LL are used as the number of places. The last bit shifted is loaded into condition code bit CC1.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
RLD		Rotate the contents of ACCU1 to the left	1	31.28	18.75	13.2	7.5
RLD	0 ... 32						
RRD		Rotate the contents of ACCU1 to the right	1	31.28	18.75	13.2	7.5
RRD	0 ... 32						
RLDA		Rotate the contents of ACCU1 one bit position to the left through condition code bit CC 1	1	31.28	18.75	13.2	7.5
RRDA		Rotate the contents of ACCU1 one bit position to the right through condition code bit CC 1	1	31.28	18.75	13.2	7.5

Status word for: **RLD, RRD, RLDA, RRDA**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	0	0	-	-	-	-	-

Accumulator Transfer Instructions, Incrementing and Decrementing

The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
CAW		Reverse the order of the bytes in ACCU1-L.	1	31.28	18.75	13.2	7.5
CAD		Reverse the order of the bytes in ACCU1.	1	31.28	18.75	13.2	7.5
TAK		Swap the contents of ACCU1 and ACCU2	1	31.28	18.75	13.2	7.5
ENT		The contents of ACCU2 and ACCU3 are transferred to ACCU3 and ACCU4.	1	31.28	18.75	13.2	7.5
LEAVE		The contents of ACCU3 and ACCU4 are transferred to ACCU2 and ACCU3.	1	31.28	18.75	13.2	7.5
PUSH		The contents of ACCU1, ACCU2 and ACCU3 are transferred to ACCU2, ACCU3 and ACCU4	1	31.28	18.75	13.2	7.5
POP		The contents of ACCU2, ACCU3 and ACCU4 are transferred to ACCU1, ACCU2 and ACCU3	1	31.28	18.75	13.2	7.5
INC	k8	Increment ACCU1-LL	1	31.28	18.75	13.2	7.5
DEC	k8	Decrement ACCU1-LL	1	31.28	18.75	13.2	7.5

Program Display and Null Operation Instructions

The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
BLD	k8	Program display instruction: Is treated by the CPU as a null operation instruction.	1	15.64	9.38	6.6	3.75
NOP	0 1	Null operation instruction	1	15.64	9.38	6.6	3.75

Data Type Conversion Instructions

The results of the conversion are in ACCU1.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
BTI		Convert contents of ACCU1-L from BCD (0 to +/- 999) to integer (16 bits) (**B**CD **T**o **I**nt)	1	31.28	18.75	13.2	7.5
BTD		Convert contents of ACCU1 from BCD (0 to +/-9 999 999) to double integer (32 bits) (**B**CD **T**o **D**oubleint)	1	31.28	18.75	13.2	7.5
DTR		Convert contents of ACCU1 from double integer (32 bits) to real number (32 bits) (**D**oubleint **T**o **R**eal)	1	62.56	37.5	26.4	15
ITD		Convert contents of ACCU1 from integer (16 bits) to double integer (32 bits) (**I**nt **T**o **D**oubleint)	1	31.28	18.75	13.2	7.5

Status word for: **BTI, BTD, DTR, ITD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Data Type Conversion Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
ITB		Convert contents of ACCU1-L from integer (16 bits) to BCD from 0 to +/- 999 (**I**nt **T**o **B**CD)	1	31.28	18.75	13.2	7.5
DTB		Convert contents of ACCU1 from double integer (32 bits) to BCD from 0 to +/- 9 999 999 (**D**oubleint **T**o **B**CD)	1	31.28	18.75	13.2	7.5

Status word for: **ITB, DTB**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	Yes	Yes	-	-	-	-

Data Type Conversion Instructions, continued

The real number to be converted is in ACCU1.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
RND		Convert a real number into a 32-bit integer.	1	31.28	18.75	13.2	7.5
RND-		Convert a real number into a 32-bit integer. The number is rounded up to the next whole number.	1	31.28	18.75	13.2	7.5
RND+		Convert a real number into a 32-bit integer. The number is rounded up to the next whole number.	1	31.28	18.75	13.2	7.5
TRUNC		Convert a real number into a 32-bit integer. The places after the decimal point are truncated.	1	31.28	18.75	13.2	7.5

Status word for: **RND, RND- RND+ TRUNC**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	Yes	Yes	-	-	-	-

Forming the Ones and Twos Complements

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
INVI		Form the ones complement of ACCU1-L	1	31.28	18.75	13.2	7.5
INVD		Form the ones complement of ACCU1	1	31.28	18.75	13.2	7.5

Status word for: **INVI, INVD**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

NEGI		Form the twos complement of ACCU1-L (integer)	1	31.28	18.75	13.2	7.5
NEGD		Form the twos complement of ACCU1 (double integer)	1	31.28	18.75	13.2	7.5

Status word for: **NEGI, NEGD,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	Yes	Yes	Yes	Yes	-	-	-	-

Block Call Instructions

The runtimes of the System Functions are specified in the chapter entitled “System Functions” as of page 20. The information on the status word only relates to the block call itself and not to the commands called in this block.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
CALL	FB q, DB q	Unconditional call of an FB, with parameter transfer	15/17[1)]	1219.73 [2)]	731.25 [2)]	488.48 [2]	292.5 [2)]
CALL	SFB q. DB q	Unconditional call of an SFB, with parameter transfer	16/17 [1)]	1219.73 [2)]	731.25 [2)]	488.48 [2)]	292.5 [2)]
CALL	FC q	Unconditional call of a function, with parameter transfer	7/8 [1)]	1063.35 [2)]	637.5 [2)]	425.85 [2)]	255 [2)]
CALL	SFCq	Unconditional call of an SFC, with parameter transfer	8	1063.35 [2)]	637.5 [2)]	425.85 [2)]	255 [2)]

Status word for: **CALL,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	0	0	1	-	0

1) The instruction length depends on the block number as of (0...255 or higher).
2) Plus time for parameter supply

Block Call Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
UC	FB q	Unconditional call of blocks,	1[1)]/2	688.05	412.5	275.55	165
	FC q	without parameter transfer		688.05	412.5	275.55	165
	FB [e]	Memory-indirect FB call	2	688.05 [+)]	412.5 [+)]	275.55 [+)]	165 [+)]
	FC [e]	Memory-indirect FC call	2	688.05[+)]	412.5 [+)]	275.55 [+)]	165 [+)]
	Parameter	FB/FC call via parameter	2	688.05 [+)]	412.5 [+)]	275.55 [+)]	165 [+)]
CC	FB q	Conditional call of blocks, without	1 [1)]/2	750.6/156.38 [2)]	270/93.75 [+)]	300/62.63 [+)]	180/37.5 [+)]
	FC q	parameter transfer		750.6/156.38 [2)]	270/93.75 [+)]	300/62.63 [+)]	180/37.5 [+)]
	FB [e]	Memory-indirect FB call	2	750.6[+]/156.38 [+2)]	270 [+]/93.75 [+ 2)]	300 [+]/62.63 [+ 2)]	180 [+]/37.5 [+ 2)]
	FC [e]	Memory-indirect FC call	2	750.6[+]/156.38 [+2)]	270 [+]/93.75 [+ 2)]	300 [+]/62.63 [+ 2)]	180 [+]/37.5 [+ 2)]
	Parameter	FB/FC call via parameter	2	750.6[+]/156.38 [+2]	270 [+]/93.75 [+ 2)]	300 [+]/62.63 [+ 2]	180 [+]/37.5 [+ 2)]

Status word for: **UC, CC,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	- [3)]	-
Instruction affects:	-	-	-	-	0	0	1	- [3)]	0

1) With direct instruction (DB) addressing; Block No. 0 to 255
+ Plus time required for loading the address of the instruction (see page 20)
2) If call is not executed
3 Instruction CC: Depending on RLO, sets RLO = 1

Block Call Instructions, continued

Instr.	Address ID	Description	Length in words	Ausführungszeit in ns							
				CPU 412-5H		CPU 414-5H		CPU 416-5H		CPU 417-5H	
				1. Open	2. - n. Open [1]	1. Open	2. - n. Open [1]	1. Open	2. - n. Open [1]	1. Open	2. - n. Open [1]
OPN		Select a data block									
	DB q DI q	Direct data block, DB Direct instance DB	1[2]/2	125.12	31.28	75.0	18.75	52.8	13.2	30	7.5
	DB [e] DI [e]	Data block, indirect save Bit memory area M Local data area L Data block DB/DI	2	125.12 125.12 187.68	62.56 62.56 93.84	75.0 75.0 112.5	37.5 37.5 56.25	52.8 52.8 79.2	26.4 26.4 39.6	30 30 45	15 15 22.5
	Param.	Data block via parameters	2	187.68	93.84	112.5	56.25	79.2	39.6	45	22.5

Status word for: **OPN,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

[1] If the same DB or DI is already selected
[2] Direct data block, DB No. 1 to 255

Block End Instructions

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
BE		End block	1	594.23	356.25	237.98	142.5
BEU		End block unconditionally	1	594.23	356.25	237.98	142.5

Status word for: **BE, BEU,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	0	0	1	-	0

BEC		End block conditionally if RLO = "1"		657.19 125.1 [1)]	394 75 [1)]	263.19 50 [1)]	157.6 30 [1)]

Status word for: **BEC,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	Yes	0	1	1	0

[1)] If jump is not executed

Exchanging Data Blocks

Exchanging the two current data blocks. The current shared data block becomes the current instance data block, and vice versa. The status word is not affected.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
CDB		Exchange data blocks	1	62.56	37.5	26.4	15

Jump Instructions

Jumping as a function of conditions.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
JU	LABEL	Jump unconditionally	2	218.93	131.25	87.68	52.5

Status word for: **JU,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

JC	MARKE	Jump if RLO = "1"	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]
JCN	MARKE	Jump if RLO = "0"	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]

Status word for: **JC, JCN,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	1	1	0

[1] If jump is not executed

Jump Instructions, continued

Ope-ration	Operand	Bedeutung	Länge in Worten	Ausführungszeit in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
JCB	LABEL	Jump if RLO = “1”. Save the RLO in the BR bit	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]
JNB	LABEL	Jump if RLO = “0”. Save the RLO in the BR bit	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]

Status word for: **JCB, JNB,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	Yes	-	-	-	-	0	1	1	0

JBI	LABEL	Jump if BR = “1”	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]
JNBI	LABEL	Jump if BR = "0"	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]

Status word for: **JBI, JNBI,**	BR	CC 1	CC 0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	Yes	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	1	-	0

[1] if jump is not executed

Jump Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
JO	LABEL	Jump on stored overflow (OV = "1")	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]

Status word for: **JO,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	Yes	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

JOS	LABEL	Jump on stored overflow (OS = "1")	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]

Status word for: **JOS,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	Yes	-	-	-	-
Instruction affects:	-	-	-	-	0	-	-	-	-

[1] If jump is not executed

Jump Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
JUO	LABEL	Jump if “unordered math instruction” (CC1=1 and CC0=1)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.5 [1]
JZ	LABEL	Jump if result = 0 (CC1=0 and CC0=0)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.1 [1]
JP	LABEL	Jump if result > 0 (CC1=1 and CC0=0)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.1 [1]
JM	LABEL	Jump if result < 0 (CC1=0 and CC0=1)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.1 [1]
JN	LABEL	Jump if result ≠ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=1)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.1 [1]
JMZ	LABEL	Jump if result ≤ 0 (CC1=0 and CC0=1) or (CC1=0 and CC0=0)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.1 [1]
JPZ	LABEL	Jump if result ≥ 0 (CC1=1 and CC0=0) or (CC1=0 and CC0=0)	2	218.93/31.28 [1]	131.25/18.75 [1]	87.68/13.2 [1]	52.5/7.1 [1]

Status word for: **JUO, JZ, JP, JM, JN, JMZ, JPZ,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	Yes	Yes	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

[1] If jump is not executed

Jump Instructions, continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
JL	MARKE	Jump distributor This instruction is followed by a list of jump instructions. The address identifier is a jump label to subsequent instructions in this list. ACCU1-LL contains the number of the jump instruction to be executed (max. 254). The number of the first jump instruction is 0.	2	218.93	131.25	87.68	52.5
LOOP	MARKE	Decrement ACCU1-L and jump if ACCU1-L ≥ 0 (loop programming)	2	187.65/31.28 [1)]	112.5/18.75 [1)]	75.15/13.2	45/7.5 [1)]

Status word for: **JL, LOOP,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

[1)] If jump is not executed

Instructions for the Master Control Relay (MCR)

MCR=1 => MCR is deactivated. MCR=0 => MCR is activated.
“T” and “=” instructions write zeros to the corresponding address identifiers if RLO = “0”; “S” and ”R” instructions leave the memory contents unchanged.

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
MCR(		Open an MCR zone. Save the RLO to the MCR stack.	1	31.28	18.75	13.2	7.5

Status word for: **MCR(,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	Yes	-
Instruction affects:	-	-	-	-	-	0	1	-	0

)MCR		Close an MCR zone. Pop an entry off the MCR stack.	1	31.28	18.75	13.2	7.5

Status word for: **)MCR,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	0	1	-	0

Instructions for the Master Control Relay (MCR), continued

Instr.	Address ID	Description	Length in words	Execution Time in ns			
				CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
MCRA		Activate the MCR	1	31.28	18.75	13.2	7.5
MCRD		Deactivate the MCR	1	31.28	18.75	13.2	7.5

Status word for: **MCRA, MCRD,**	BR	CC1	CC0	OV	OS	OR	STA	RLO	/FC
Instruction depends on:	-	-	-	-	-	-	-	-	-
Instruction affects:	-	-	-	-	-	-	-	-	-

Oganization Blocks (OB)

A user program for the S7-400 is made up of blocks containing the statements, parameters and data for the relevant CPU. The number of blocks you can create or which are provided by the operating system is different for each of the S7-400 CPUs. You will find a detailed description of the OBs and their use in the *STEP 7 V 5.4 Programming Manual*.

Organization Blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H	Start Events (Hexadecimal value)
Free cycle:					
OB 1	x	x	x	x	1101, 1102, 1103, 1104, 1105
Time-of-day interrupts:					
OB 10	x	x	x	x	1111
OB 11	x	x	x	x	1112
OB 12	x	x	x	x	1113
OB 13	x	x	x	x	1114
OB 14			x	x	1115
OB 15			x	x	1116
OB 16			x	x	1117
OB 17			x	x	1118

Organization Blocks (OB), continued

Organzation Blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H	Start Events (Hexadecimal Value)
Time-delay interrupts:					
OB 20	x	x	x	x	1121
OB 21	x	x	x	x	1122
OB 22	x	x	x	x	1123
OB 23	x	x	x	x	1124
Timed interrupts:[1]					
OB 30			x	x	1131
OB 31			x	x	1132
OB 32	x	x	x	x	1133
OB 33	x	x	x	x	1134
OB 34	x	x	x	x	1135
OB 35	x	x	x	x	1136
OB 36			x	x	1137
OB 37			x	x	1138
OB 38			x	x	1139

[1] Additional start event of the H-CPUs for OB 30 to OB 38: 1130_H

Organization Blocks (OB), continued

Organization Blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H	Start Events (Hexadecimal value)
Hardware interrupts:					
OB 40	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 41	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 42	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 43	x	x	x	x	1141, 1142, 1143, 1144, 1145
OB 44			x	x	1141, 1142, 1143, 1144, 1145
OB 45			x	x	1141, 1142, 1143, 1144, 1145
OB 46			x	x	1141, 1142, 1143, 1144, 1145
OB 47			x	x	1141, 1142, 1143, 1144, 1145
Interrupt OBs for DPV1:					
OB 55	x	x	x	x	1155

Organization Blocks (OB), continued

Organization blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H	Start events (Hexadecimal value)
Redundancy error interrupts:					
OB 70	x	x	x	x	73A2, 73A3, 72A3
OB 72	x	x	x	x	7301, 7302, 7303, 7320, 7321, 7322, 7323, 7331, 7333, 7334, 7335, 7340, 7341, 7342, 7343, 7344, 7950, 7951, 7952, 7852, 7953, 7954, 7955, 7855, 7956, 73C1, 73C2
Asynchronous error interrupts:					
OB 80	x	x	x	x	3501, 3502, 3505, 3506, 3507, 3508, 3509, 350A
OB 81	x	x	x	x	3821, 3822, 3823, 3825, 3826, 3827, 3831, 3832, 3833, 3921, 3922, 3923, 3925, 3926, 3927, 3931, 3932, 3933
OB 82	x	x	x	x	3842, 3942
OB 83	x	x	x	x	3951, 3954, 3854, 3855, 3856, 3858, 3861, 3961, 3863, 3864, 3865, 3866, 3966, 3267, 3367, 3968
OB 84	x	x	x	x	3582, 3583, 3986, 3587
OB 85	x	x	x	x	35A1, 35A2, 35A3, 34A4, 35A4, 39B1, 39B2, 38B3, 39B3, 38B4, 39B4
OB 86	x	x	x	x	38C1, 39C1, 38C2, 39C3, 38C4, 39C4, 38C5, 39C5, 38C6, 38C7, 38C8, 39CA, 38CB, 39CB, 38CC, 39CD, 39CE
OB 87	x	x	x	x	35D2, 35D3, 35D4, 35D5, 35E1, 35E2, 35E3, 35E4, 35E5, 35E6
OB 88	x	x	x	x	3573, 3575, 3576

Organization Blocks (OB), continued

Organization Blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H	Start Events (Hexadecimal value)
Warm restart:					
OB 100	x	x	x	x	1381, 1382, 138A, 138B
Cold restart:					
OB 102	x	x	x	x	1385, 1386, 1387, 1388
Synchronous error interrupts:					
OB 121	x	x	x	x	2521, 2522, 2523, 2524, 2525, 2526, 2527, 2528, 2529, 2530, 2531, 2532, 2533, 2534, 2535, 253A, 253C, 253D, 253E, 253F
OB 122	x	x	x	x	2942, 2943, 2944, 2945

Function Blocks (FB)

The following tables list the quantities, numbers and maximum sizes of the function blocks you can create for the various S7-400 CPUs.

Function Blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
Quantity	3000	3000	8000	8000
Permitted numbers	0 to 7999	0 to 7999	0 to 7999	0 to 7999
Maximum size of a function block (code required for execution)	64 KByte	64 KByte	64 KByte	64 KByte

Functions (FC) and Data Blocks (DB)

The following tables list the quantities, numbers and maximum sizes of the functions and data blocks you can create for the various S7-400 CPUs.

Functions	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
Quantity	3000	3000	8000	8000
Permitted numbers	0 to 7999	0 to 7999	0 to 7999	0 to 7999
Maximum size of a function (code required for execution)	64 KByte	64 KByte	64 KByte	64 KByte

Data blocks	CPU 412-5H	CPU 414-5H	CPU 416-5H	CPU 417-5H
Quantity	6000	6000	16000	16000
Permitted numbers	1 to 16000	1 to 16000	1 to 16000	1 to 16000
Maximum size of a data block (number of data bytes)	64 KByte	64 KByte	64 KByte	64 KByte

System Functions

The following tables show the system functions which are provided by the operating system of the S7-400 CPUs and the execution times for the various CPUs. (X: function available, execution times not yet available before printing).

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
0	SET_CLK	Set clock	131	368	83	221	54	157	34	96
1	READ_CLK	Read clock	8	45	7	30	5	23	3	11
2	SET_RTM	Set run-time meter	8	8	7	7	5	5	2	2
3	CTRL_RTM	Start and stop run-time meter	7	7	5	5	4	4	2	2
4	READ_RTM	Read run-time meter	8	38	5	23	3	18	2	6
5	GADR_LGC	Find logical address of a channel Rack 0	15	15	8	8	5	5	3	3
		internal DP	16	16	13	13	7	7	4	4
6	RD_SINFO	Read start information of current OB	9	9	7	7	6	6	3	3
9	EN_MSG	Enable block-related, symbol-related, and group status messages. First call, REQ = 1	46	101	30	75	19	51	11	27
		Last call	14	45	7	29	5	23	3	10
10	DIS_MSG	Disable block-related, symbol-related, and group status messages. First call, REQ = 1	46	107	32	74	17	48	11	27
		Last call	14	44	7	30	5	23	3	10

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
13	DPNRM_DG	Read slave diagnostic data First call	77	122	46	78	31	49	20	28
		Intermediate call	30	30	20	20	13	13	7	7
		Last call (28 bytes)	38	38	23	23	16	16	9	9
14	DPRD_DAT	Read consistent user data (n bytes)via integrated DP interface 3 bytes	31	70	17	48	11	35	8	19
		via integrated DP interface 32 bytes	32	71	18	49	12	36	8	24
		via external DP interface 3 bytes	53	61	34	40	24	37	16	25
		via external DP interface 32 bytes	107	163	66	105	45	73	36	42
		via integrated PROFINET interface 8 bytes	31	72	18	49	12	36	9	19
		via integrated PROFINET interface 32 bytes	32	73	19	50	13	37	9	24
15	DPWR_DAT	Write consistent user data (n bytes)via integrated DP interface 3 bytes	37	76	25	50	14	36	10	16
		via integrated DP interface 32 bytes	38	77	26	51	15	37	11	19
		via external DP interface 3 bytes	60	82	34	54	25	43	14	26
		via external DP interface 32 bytes	130	147	81	84	63	70	42	54
		Write consistent user data using integrated PROFINET interface 8 bytes	37	76	24	46	14	32	12	18
		via integrated PROFINET interface 32 bytes	38	77	25	48	15	35	13	22

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
17	ALARM_SQ [1]	Generate acknowledgeable block-related messages. First call, SIG = 0 -> 1	140 - 302	299 - 502	93 - 189	206 - 350	71 - 155	144 - 272	53 - 120	89 - 167
		Empty call	68 - 199	155 - 252	68 - 130	120 - 296	54 - 114	92 - 208	37 - 99	57 - 111
18	ALARM_S [1]	Generate unacknowledgeable block-related messages.First call, SIG = 0 -> 1	121 - 312	338 - 452	70 - 191	219 - 312	48 - 158	145 - 240	29 - 125	88 - 168
		Empty call	45 - 202	130 - 249	24 - 132	81 - 155	17 - 115	54 - 134	10 - 98	32 - 112
19	ALARM_SC [1]	Generate acknowledgeable block-related messages.	30 - 195	106 - 255	17 - 135	68 - 158	11 - 117	46 - 135	9 - 100	28 - 112
20	BLKMOV	Copy variable within work memory (n = number of bytes to be copied)	16 + n * 0,052	16 + n * 0,052	13 + n * 0,036	13 + n * 0,036	7 + n * 0,025	7 + n * 0,025	4 + n * 0,016	4 + n * 0,016
		Source = Load memory	16 +n * 0,052	16 +n * 0,052	14 +n * 0,036	14 +n * 0,036	7 + n * 0,025	7 + n * 0,025	5 +n * 0,016	5 +n * 0,016
21	FILL	Prefill field within work memory (n = length of target variable in bytes)	15 + n * 0,025	15 + n * 0,025	8 + n * 0,016	8 + n * 0,016	6 + n * 0,012	6 + n * 0,012	3 + n * 0,01	3 + n * 0,01

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
22	CREAT_DB	Create data block	54 + n * 0,06	206 + n * 0,06	31 + n * 0,04	134 + n * 0,04	20 + n * 0,03	90 + n * 0,03	13 + n * 0,02	51 + n * 0,02
		Save last free DB No. from field of 100 DBs	353	500	215	313	142	204	89	125
23	DEL_DB	Delete data block	69	436	40	273	26	188	17	117
24	TEST_DB	Test data block	25	167	15	115	9	80	6	44
25	COMPRESS	Compress user memory First call (Trigger)	39	135	25	80	17	52	11	30
		Subsequent call	8	8	6	6	4	4	2	2
26	UPDAT_PI	Update process image input table (run-time entry for 1 DI 32 in the central rack)	15	39	13	29	11	22	9	12
		AI 8 * 13Bit	31	138	30	97	29	71	29	51
27	UPDAT_PO	Ausgänge aktualisieren (Laufzeitangabe für 1 DO 32 im ZG)	16	45	11	29	9	22	9	13
		AO 8 * 13 Bit	31	138	30	97	27	67	26	49
28	SET_TINT	Set time-of-day interrupt	29	61	15	38	9	27	6	15
29	CAN_TINT	Cancel time-of-day interrupt	61	346	37	220	23	151	15	92
30	ACT_TINT	Activate time-of-day interrupt	22	53	9	36	7	28	5	13
31	QRY_TINT	Query time-of-day interrupt	7	7	6	6	3	3	1	1
32	SRT_DINT	Start time-delay interrupt	14	14	9	9	6	6	3	3
33	CAN_DINT	Cancel time-delay interrupt	9	9	8	8	5	5	3	3
34	QRY_DINT	Query time-delay interrupt	7	7	6	6	4	4	1	1
36	MSK_FLT	Mask synchronous faults	7	7	5	6	4	4	2	2

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
37	DMSK_FLT	Demask synchronous faults	7	7	6	6	4	4	2	2
38	READ_ERR	Read error register	7	7	6	6	4	4	2	2
39	DIS_IRT	Discard new events Block all events (MODE = 0)	55	55	37	37	24	24	16	16
		Block all events of a priority class (MODE = 1)	15	15	8	8	6	6	4	4
		Block one event (MODE = 2)	9	9	6	6	4	4	2	2
40	EN_IRT	Stop discarding events Enable all events (MODE = 0)	52	52	31	31	21	21	14	14
		Enable all events in a priority class (MODE = 1)	15	15	8	8	6	6	4	4
		Enable an event (MODE = 2)	9	9	6	6	4	4	2	2
41	DIS_AIRT	Delay interrupt events the first time delay is activated [1]	47	47	30	30	20	20	12	12
		if the delay is already activated	7	7	5	5	3	3	1	1

[1] When activating the delay for the first time, the SFC 41 runtime depends on the priority class in which the SFC 41 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
42	EN_AIRT	if other delays are present	8	8	6	6	4	4	2	2
		Stop delaying interrupt eventswhen canceling the last delay [1]	107	107	67	67	46	46	28	28
43	RE_TRIGR	Retrigger cycle monitoring time	53	300	31	184	19	135	14	82
44	REPL_VAL	Transfer substitute value to ACCU 1	8	8	6	6	4	4	2	2
46	STP	Force CPU into STOP mode cannot be measured	--	--	--	--	--	--	--	--
47	WAIT	Delay program execution in addition to waiting time	7	7	6	6	4	4	2	2
48	SNC_RTCB	Synchronize slave clocks	7	37	5	23	4	18	2	9
49	LGC_GADR	Find slot with logical address	15	15	13	13	7	7	4	4
50	RD_LGADR	Find all logical addresses of a block (run-time entry for 1 DI 32 in the central rack)	32	32	22	22	14	14	8	8

[1] When cancelling the last delay, the SFC 42 runtime depends on the priority class in which the SFC 42 is called. The specified runtime refers to the call in OB 1. It decreases while the priority class number increases.

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	"Module identification" partial list Display one data record (0111)	33	105	23	63	15	49	9	38
51	RDSYSST	"Module Identification" partial list Display all data records (0012)	74	74	39	40	26	26	16	16
		Display one data record (0112)	44	44	23	23	16	16	10	10
		Display header information (0F12)	30	30	16	16	10	10	7	7
51	RDSYSST	"Save" partial listDisplay header information (0113)	38	38	23	23	15	15	9	9
51	RDSYSST	"System Areas" partial list Display all data records (0014)	44	44	24	24	16	16	9	9
		Display header information (0F14)	30	30	17	17	10	10	7	7
51	RDSYSST	"Block Types" partial list Display all data records (0015)	44	44	23	23	15	15	9	9
51	RDSYSST	"Status of Module LEDs" partial list Display status of all LEDs (0019)	68	--	55	--	38	--	23	--
		Display header information (0F19)	40	--	24	--	16	--	10	--
51	RDSYSST	"Component Identification" partial list Display all components (001C)	62	189	38	141	27	122	18	107
		Display one of the components (011C)	41	167	29	131	17	114	12	102
		Display all components of a H-system CPU (021C)	63	183	38	141	27	110	18	107
		Display a component of all redundant CPUs of the H-system (031C)	41	175	29	133	17	117	11	101
		Display header information (0F1C)	33	159	22	125	15	110	9	98

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	"Interrupt status" partial list Display one data record (0222)	45	45	29	29	17	17	11	11
51	RDSYSST	"TPA /CPU assignment" partial list Assignment between all process image partitions and OBs (0025)	97	97	55	55	37	37	22	22
		Assignment between a process image partition and the corresponding OB (0125)	37	37	23	23	14	14	8	8
51	RDSYSST	"Status information communication" partial list Display status information of a communication unit (0132)	41 – 71	76 – 337	29 – 45	51 – 212	16 – 30	27 – 140	11 – 17	18 – 90
		"Status information communication" partial list Display status information of a communication unit (0232)	63	191	39	114	25	79	16	52
51	RDSYSST	"H-CPU group information" partial list Current status of the H system (0071)	-	68	-	44	-	29	-	16
		Header information (0F71)	-	30	-	21	-	10	-	7
51	RDSYSST	"Modules LEDs" partial list Status of an LED (0174)	47	83	29	52	17	28	11	19

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	"Switched DP slaves in the H system" partial list (0075)	-	2509	-	1501	-	997	-	602
		Communication status between the H system and a switched DP slave (0C75)	-	125	-	74	-	62	-	51
		Header information (0F75)	-	2219	-	1340	-	890	-	540
51	RDSYSST	"Module status information" partial list Central a module with logical basic address (0090)	95	95	60	60	39	39	25	25
		a DP master system (0190)	39	39	29	29	14	14	9	9
		Header information (0F90)	30	30	18	18	10	10	7	7
51	RDSYSST	Partial list "Component status information" All submodules of the host module (0591)	54	213	31	145	22	113	13	91
		Central at a module using the logical basic address (0C91)	56	130	38	83	24	56	15	35
		Distributed at integrated DP interface of a module using the logical basic address (0C91)	71	146	45	91	29	63	17	39
		Distributed at integrated PROFINET interface of a module using the logical basic address (0C91)	62	130	38	83	24	56	15	35
		all PROFINET IO systems (0A91)	86	153	54	98	37	60	21	39

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	"Module status information" partial listof a module (distributed) with logical basic address (4C91) First call	80	153	53	98	33	63	25	39
		Intermediate call	52	52	30	30	18	18	16	16
		Last call	59	59	36	36	22	22	17	17
51	RDSYSST	Parts list "Component status information" All modules in the specified rack (n=number of DS) (0D91)	71 + n* 18	176 + n* 20	46 + n * 16	114 + n * 16	30 + n * 14	75 + n * 14	18 + n * 10	50 + n * 12
		All modules in the specified DP station (0D91)	57- 77	161 - 191	38 - 46	105 - 114	24 – 31	68 - 81	15 - 19	46 - 53
		All modules in the specified PNIO station (0D91)	137	230	82	159	54	106	34	76
51	RDSYSST	"Rack/station status information" partial list central Display setpoint status of rack 0 (0092)	33	76	23	50	15	27	9	17
		distributed Display setpoint status of DP system 1 (0092)	162	206	99	122	67	76	39	50
51	RDSYSST	Readout of setpoint status of DP system 1 (using external DP interface) (4092)	64	130	39	84	29	52	16	33

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	Display activation status of DP master system 1 (via integrated DP interface) (0192)	223	241	141	163	102	115	61	67
51	RDSYSST	central Display the actual status of rack 0 (0292)	33	75	23	45	15	26	9	17
		distributed Display the actual status of DP system 1 (0292)	164	207	101	128	69	81	41	48
51	RDSYSST	Display the actual status of the stations of a DP master system (via external DP interface) (4292)	69	129	39	84	28	51	16	33
51	RDSYSST	Display the status of rack 0 battery buffer if at least one battery has failed (0392)	33	75	23	45	15	26	9	17

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	Display the status of the entire battery buffer of a CPU (0492)	33	75	23	45	15	27	9	17
51	RDSYSST	Display the status of the 24 V supply of all racks of a CPU (0592)	33	75	23	44	15	29	9	17
51	RDSYSST	Central Display the diagnostic status of the expansion devices (0692)	71	114	46	68	31	41	18	26
51	RDSYSST	Distributed Display the diagnostic status of the DP system 1 stations (via integrated DP interface) (0692)	194	237	117	144	78	91	48	58
51	RDSYSST	Diagnostic status of the stations of a DP master system connected via an external DP interface (4692) First call	69	129	39	83	28	52	16	33
		Intermediate call	38	38	27	27	15	15	9	9
		Last call	46	46	29	29	17	17	11	11

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
51	RDSYSST	Parts lits "Diagnostic data DP slave" Display using configured diagnostic address (00B4) First call	87	136	55	82	38	52	23	31
		Intermediate call, REQ = 0 (00B4)	52	52	34	34	18	18	11	11
		Last call (6 – 240 bytes) (00B4)	72	72	51	51	31	31	19	19
52	WR_USMSG	Write user entry in diagnostic buffer with message	39	57	23	53	15	36	9	17
		Without message	29	49	22	51	14	32	9	19
54	RD_DPARM	Read dynamic parameters central AI 8 * 13 bits	46	70	29	44	17	29	11	14
		Distributed AI 8 * 12 bits (DS1 = 14 bytes)	53	53	32	36	22	22	13	16
55	WR_PARM	Write dynamic parameters central AI 8 * 13 bits	138	192	100	136	79	102	63	73
		distributed First call AI 8 * 12 bits (14 - 240 bytes)	92	130	54	83	38	52	22	31
		Distributed Intermediate/last call, REQ = 0	45	45	29	29	19	19	10	10
56	WR_DPARM	Write predefined dynamic parameters AI 8*13 bits central	184	238	138	169	119	141	100	110
		Distributed First call AI 8 * 12 bits (2 - 240 bytes)	77	108	46	68	31	49	19	27
		Intermediate/last call	38	38	23	23	16	16	9	9

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
57	PARM_MOD	Assign module parameters localModule/DS number/DS lengths in bytesAI 8*13 bits	316	385	232	283	204	241	175	192
		distributedAO 8*12 bits First call (16-240 bytes)	71	108	46	68	31	52	19	27
		distributed Intermediate/last call	38	38	23	23	15	15	9	9
58	WR_REC	Write parameter data record local (n = number of bytes)	97 + n * 2.6	129 + n * 2.6	71 + n * 2.4	90 + n * 2.4	55 + n * 2.3	79 + n * 2.3	40 + n * 2.2	69 + n * 2.2
		First call, integrated DP interface module (n = number of bytes)	84 + n * 0.06	121 + n * 0.06	47 + n * 0.06	71 + n * 0.06	32 + n * 0.05	47 + n * 0.05	20 + n * 0.04	32 + n * 0.04
		Intermediate call, REQ = 0 integrated DP interface module	36	36	17	17	12	12	8	8
		Last call, integrated DP interface module	37	37	18	18	14	14	8	8
		First call, external DP interface module (n = number of bytes)	84 + n * 0.06	121 + n * 0.06	47 + n * 0.06	71 + n * 0.06	32 + n * 0.04	52 + n * 0.05	20 + n * 0.03	32 + n * 0.03
		Intermediate call, REQ = 0 external DP interface module	36	36	17	17	11	11	8	8
		Last call, external DP interface module	37	37	21	21	14	14	8	8

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
59	RD_REC	Read data record local (n = number of bytes)	110 + n * 2.8	151 + n * 2.8	73 + n * 2.4	95 + n * 2.4	56 + n * 2.4	81 + n * 2.4	40 + n * 2.3	72 + n * 2.4
		First call, integrated DP interface module	77	121	52	77	32	51	20	32
		Intermediate call, REQ = 0 integrated DP interface module	37	37	17	17	11	11	8	8
		Last call, integrated DP interface module (n = number of bytes)	67 + n * 0.7	67 + n * 0.7	38 + n * 0.4	38 + n * 0.4	25 + n * 0.2	26 + n * 0.2	16 + n * 0.13	17 + n * 0.13
		First call, external DP interface module	77	121	52	77	32	52	20	32
		Intermediate call, REQ = 0 external DP interface module	37	37	17	17	11	11	8	8
		Last call, external DP interface module (n = number of bytes)	67 + n * 0.1	67 + n * 0.1	38 + n * 0.07	38 + n * 0.07	25 + n * 0.05	26 + n * 0.05	16 + n * 0.02	17 + n * 0.02
62	CONTROL	Check status of the connection belonging to a local communication-SFB-instance	38	70	19	51	15	32	8	18
64	TIME_TCK	Display millisecond timer	7	31	3	23	2	15	2	5
70	GEO_LOG	Determining the start address of a module using the slot	15	15	13	13	7	7	4	4
71	LOG_GEO	Determining the module slot associated with a logical address	16	16	14	14	8	8	4	4
78	OB_RT	Determining the OB Program Runtime	16	46	10	29	7	20	4	10
79	SET	Set bit array in I/O area	15 +n *	39 +n * 3.7	10 + n *	28 +n * 2.5	7 + n *	19 + n *	5 +n *	10 +n * 1.3

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
		n = number of bits to set at 1	1.0		0.7		0.55	1.8	0.4	
80	RSET	Delete bit array in I/O area n = number of bits to set at 0	15 + n * 1.0	39 + n * 3.8	10 + n * 0.7	28 + n * 2.5	7 + n * 0.55	19 + n * 1.8	5 + n * 0.4	10 + n * 1.3
81	UBLKMOV	Copy variable without interruption n = number of bytes to copy	14 + n* 0.04	14 + n* 0.05	8 + n* 0.03	8 + n* 0.03	5 + n * 0.025	5 + n * 0.025	3 + n* 0.02	3 + n* 0.02
87	C_DIAG	Determine current connection status MODE = 0	9	61	8	37	4	24	3	11
		Mode = 1, 2, 3	130	607	78	380	50	253	32	158
90	H_CTRL	Influence processes involving fault-tolerant systems	7	7	6	6	4	4	2	2
100	SET_CLKS	Set clock and clock status MODE = 1	122	361	76	228	49	152	31	97
		MODE = 2	77	354	47	222	31	144	20	94
		MODE = 3	124	361	42	228	49	160	31	99
101	RTM	Handle operating hour meter Mode = 0 Read	16	45	9	29	7	20	4	8
		Mode = 1, 2 Start/Stop	16	45	9	29	7	20	4	8
		Mode = 4, 5, 6 Set	16	45	9	29	7	20	4	8
103	DP_TOPOL	Detemine bus topology in a DP master system first call, REQ = 1	82	200	46	122	31	84	18	48
		Intermediate call	15	15	8	8	6	6	3	3
		Last call BUSY = 0	15	15	12	12	9	9	4	4

SFC No.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
104	CIR	Controls the CiR procedure MODE = 0, Information	10	-	5	-	4	-	3	-
		MODE = 1, Enable CiR procedure	10	-	5	-	4	-	3	-
		MODE = 2, Disable CiR procefure entirely	10	-	5	-	4	-	3	-
		MODE = 3, Disable CiR procedure partially	10	-	5	-	4	-	3	-
105	READ_SI	Read dynamically assigned system resources MODE = 0	38 - 822 1)	107 - 822 1)	23 - 500 1)	122 - 507 1)	16 - 406 1)	170 - 411 1)	10 - 260 1)	236 - 257 1)
		MODE = 1	46 - 968 2)	207 - 1129 2)	31 - 638 2)	181 - 797 2)	19 - 653 2)	267 - 902 2)	12 - 413 2)	232 - 636 2)
		MODE = 2	46 - 1021 2)	198 - 1183 2)	31 - 976 2)	180 - 1129 2)	19 - 2034 2)	266 - 2284 2)	12 - 1246 2)	233 - 1462 2)
		MODE = 3	46 - 944 3)	207 - 1089 3)	31 - 622 3)	180 - 788 3)	19 – 913 3)	266 – 1155 3)	12 - 559 3)	233 - 776 3)
106	DEL_SI	Enable dynamically assigned system resources MODE = 1 2)	69 - 2848 1)	399 - 24229 1)	40 - 2741 1)	353 - 23094 1)	29 - 4900 1)	541 - 25887 1)	16 - 2999 1)	491 - 25256 1)
		MODE = 2 2)	64 - 776 1)	383 - 1114 1)	40 - 722 1)	354 - 1035 1)	26 - 1481 1)	551 - 2021 1)	16 - 890 1)	495 - 1381 1)
		MODE = 3 3)	69 - 2848 2)	400 - 23392 2)	40 - 2742 2)	361 - 23076 2)	26 – 4898 2)	551 – 25883 2)	16 - 2999 2)	492 - 25153 2)

1) Depending on the size of the SYS_INST target area and on the number of the system resources to be read
2) Depending on the number of active messages (assigned system resources
3) Depending on the number of active messages (assigned system resources) and on the number of assigned instances with the desired CMP_ID.

SFCNo.	SFC Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
107	ALARM_DQ	Acknowledgeable block-related messages create first call, SIG = 0 -> 1	107 - 311 [1]	222 - 552 [1]	61 - 195 [1]	144 - 312 [1]	41 – 162 [1]	98 - 243 [1]	26 - 125 [1]	60 - 168 [1]
		Call without message	37 -203 [1]	107 - 288 [1]	23 - 127 [1]	76 - 167 [1]	15 – 113 [1]	50 - 141 [1]	9 - 99 [1]	30 - 115 [1]
108	ALARM_D	Not acknowledgeable block-related messages create first call, SIG = 0 -> 1	120 - 313 [1]	242 - 587 [1]	63 - 190 [1]	148 - 291 [1]	45 – 165 [1]	102 – 255 [1]	33 - 127 [1]	69 - 165 [1]
		Call without message	38 - 204 [1]	96 - 275 [1]	19 - 127 [1]	69 - 160 [1]	15 – 105 [1]	47 – 138 [1]	9 - 102 [1]	25 - 112 [1]
109	PROTECT	Activating write protection	7	7	6	6	4	4	1	1

System Function Blocks

The following table lists the system function blocks provided with the operating system of the S7-400 CPUs as well as the execution times of the individual CPUs.

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
0	CTU	Count up	6	6	2	2	1	1	1	1
1	CTD	Count down	6	6	2	2	1	1	1	1
2	CTUD	Count up and down	6	6	2	2	1	1	1	1
3	TP	Generate pulse	7	52	2	26	2	16	2	13
4	TON	Generate on–delay	8	52	6	31	5	18	2	13
5	TOF	Generate off–delay	7	21	5	7	2	6	1	5
8	USEND	Send data without coordination (one send parameter supplied) JOB activated (1-440 bytes)	109	224	70	147	51	91	30	64
		JOB checked	39	84	23	48	16	27	9	24
		JOB finished (DONE = 1)	39	97	23	55	16	27	9	25
9	URCV	Receive data without coordination (one receive parameter supplied) JOB activated	38	91	22	55	15	27	8	24
		JOB checked	38	77	22	47	15	25	8	23
		JOB finished (NDR = 1; 1-440 bytes)	70	131	45	78	31	44	20	36
12	BSEND	Send data block by block JOB activated (1-3000 bytes)	100	190	60	116	39	66	23	46
		JOB checked	45	84	23	48	17	31	10	25
		JOB finished (DONE = 1)	45	98	23	55	17	31	10	25

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
13	BRCV	Receive data block by block JOB activated (1-3000 bytes)	47	99	30	62	22	31	12	27
		JOB checked	47	92	29	55	18	29	11	26
		JOB finished	40	97	24	55	17	29	10	26
14	GET	Read data from remote CPU (one area specified) JOB activated	91	169	53	102	34	60	20	44
		JOB checked	39	84	23	48	16	28	9	25
		JOB finished (NDR = 1; 1 – 450 bytes)	71	130	47	79	32	44	20	36
15	PUT	Write data to remote CPU JOB activated (1 – 404 bytes)	122	231	70	147	51	96	30	65
		JOB checked	39	84	23	49	16	28	9	24
		JOB finished (DONE = 1)	39	91	23	54	16	28	9	24
16	PRINT	Send data to a printer JOB activated, REQ = 1	124	259	70	155	53	96	32	66
		JOB checked	39	83	23	47	16	29	9	24
		JOB finished, DONE = 1	39	91	23	54	16	29	9	24
19	START	Start remote device JOB activated, REQ = 1	115	200	68	118	46	72	27	53
		JOB checked	45	84	23	48	16	27	9	25
		JOB finished, DONE = 1	40	91	23	54	17	32	10	29
20	STOP	Stop remote device JOB activated, REQ = 1	115	191	68	115	45	68	26	48
		JOB checked	45	84	24	47	16	30	9	25
		JOB finished, DONE = 1	45	83	24	54	16	30	9	25

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
21	RESUME	Restart remote device JOB activated, REQ = 1	115	191	68	118	46	67	27	50
		JOB checked	45	91	24	54	16	28	10	26
		JOB finished, DONE = 1	45	91	24	54	16	28	10	26
22	STATUS	Query status of remote partner JOB activated, REQ = 1	69	154	45	94	30	53	16	41
		JOB checked	39	91	23	48	16	28	9	24
		JOB finished, NDR = 1	108	160	62	88	42	56	25	41
23	USTATUS	Receive status of remote device without coordination JOB activated, NDR = 1	38	77	22	54	15	27	8	24
		JOB checked	38	77	21	54	15	27	8	23
		JOB finished	108	160	62	94	42	54	25	41
31	NOTIFY_8P	Generate block-related message without acknowledgment First call or JOB activated, SIG = 0-> 1 (1 – 420 bytes)	146	297	102	175	58	114	37	78
		JOB checked	54	96	32	55	19	30	12	27
		JOB finished, DONE = 1	54	100	32	60	19	30	12	27
32	DRUM	Implement sequencer	9	46	7	39	3	25	2	18
33	ALARM	Generate block–related message with acknowledgment First call or JOB activated, SIG = 0-> 1 (1 – 420 bytes)	146	292	89	183	61	113	37	79
		JOB checked	54	99	31	56	22	30	12	28
		Restart remote device JOB activated, REQ = 1	55	108	31	70	23	30	13	28

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
34	ALARM_8	Generate block–related message without accompanying values for 8 signals First call or JOB activated, SIG = 0-> 1 (1 – 420 bytes)	108	228	67	145	42	85	26	61
		JOB checked	54	92	30	56	19	35	12	28
		JOB finished, DONE = 1	54	107	30	63	23	37	12	29
35	ALARM_8P	Generate block–related message with accompanying values for 8 signals First call or JOB activated, SIG = 0-> 1 (1 – 420 bytes)	139	299	89	179	56	113	36	80
		JOB checked	54	98	30	55	19	30	12	27
		JOB finished, DONE = 1	54	100	30	62	23	34	12	28
36	NOTIFY	Generate block–related message without acknowledgment First call or JOB activated, SIG = 0-> 1 (1 – 420 bytes)	146	304	89	192	59	118	37	80
		JOB checked	54	92	31	55	19	31	12	27
		JOB finished, DONE = 1	54	114	31	55	19	31	12	27
37	AR_SEND	Send archive data First call or JOB activated, REQ = 1 (1 – 3000 bytes)	107	264	68	123	44	65	26	60
		JOB checked	46	101	25	56	17	33	10	26
		JOB finished, DONE = 1	46	101	25	56	17	33	10	26

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
52	RDREC	Read data record from central module	121	183	76	102	63	75	42	58
52	RDREC	Read data record from a DP slave viaintegrated DP interface, First call (2–16 bytes)	93	137	53	72	38	44	24	36
		Intermediate call	39	39	22	23	15	16	8	10
		Last call	39	44	23	31	16	17	9	11
52	RDREC	Read data record from a DP slave viaexternal DP interface, First call (4–16 bytes)	93	139	45	66	32	35	18	20
		Intermediate call	39	39	22	22	15	16	8	9
		Last call	40	44	23	23	16	17	9	10
52	RDREC	Read data record from IO device integrated PROFINET interface, First call (2-16 bytes)	84	131	47	89	32	56	19	28
		Intermediate call	37	38	22	30	14	17	8	9
		Last call	38	39	22	31	15	21	8	9
53	WRREC	Central	114	145	70	88	53	60	38	50
53	WRREC	Write data record in a DP slalve viaintegrated DP interface, First call (1–10 bytes)	93	137	54	73	37	44	24	35
		Intermediate call	39	39	23	23	15	18	8	10
		Last call	39	53	23	41	16	18	9	10
53	WRREC	Write data record in a DP slave viaexternal DP interface, First call (2–14 bytes)	93	137	51	72	33	37	18	24
		Intermediate call	39	39	22	22	15	15	8	9
		Last call	39	46	23	23	15	15	9	10

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
53	WRREC	Write data record to IO device integrated PROFINET interface, First call (1-10 bytes)	90	138	58	88	36	57	21	31
		Intermediate call	37	38	22	30	14	18	8	11
		Last call	37	38	22	31	15	21	8	11
54	RALRM	Receive interrupt Runtime measurement for non–I/O–dependent OBs, MODE = 1, OB 1	30	71	16	49	13	31	8	19
54	RALRM	Receive interrupt Runtime measurement at central IO, MODE = 1, OB 40, OB 82, OB 83, OB 86	71	123	51	69	32	47	19	31
54	RALRM	Receive interrupt Runtime measurement at integrated DP interface, MODE = 1, OB 40, OB 83, OB 86	92	177	53	120	34	75	21	55
		OB 55 to OB 57, OB 82	96	183	56	126	37	79	23	58
		OB 70	94	179	54	122	35	77	22	56
54	RALRM	Receive interrupt Runtime measurement at external DP interface, MODE = 1, OB 40, OB 83, OB 86	170	307	122	201	91	141	68	100
		OB 55 to OB 57, OB 82	216	345	176	248	137	186	107	141
		OB 70	177	322	131	215	97	150	75	110
54	RALRM	Receive interrupt Runtime measurement at integrated PROFINET interface, MODE = 1, OB 40, OB 83, OB 86	99	307	67	267	46	223	33	199
		OB 82	104	322	71	281	49	234	35	205
		OB 70	101	310	68	269	47	226	34	202

SFB No.	SFB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
81	RD_DPAR	Read predefined parameters centrally	77	155	47	100	31	70	19	40
		Read predefined parameters internal DP	77	106	47	69	31	49	19	35
		Read predefined parameters external DP First call	84	115	60	70	35	53	24	35
		Last call	84	151	60	85	35	54	24	38
		Read predefined parameters internal PNIO First call	107	231	63	223	40	80	26	48
		Intermedidate call	107	246	74	122	48	74	28	51
		Last call	39	70	24	45	26	32	10	18

Function blocks for open communication via Industrial Ethernet

The following tables list the function blocks for open communication via Industrial Ethernet that are made available by the operating system of the S7-400-CPUs as well as the execution times on the respective CPU.

FB No.	FB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
63	TSEND	Send data via TCP and ISO on TCP (n bytes)								
		First call	85 + n*0.014	230 + n*0.016	53 + n*0.01	152 + n*0.01	34 + n*0.008	100 + n*0.008	21 + n*0.008	65 + n*0.008
		Intermediate call	32	108	23	69	15	50	9	33
		Last call	32	108	23	69	15	51	9	33
64	TRCV	Receive data via TCP and ISO on TCP (n bytes)								
		First call	77	178 + n*0.016	46	115 + n*0.01	31	78 + n*0.008	19	51 + n*0.008
		Intermediate call	39	108	23	69	15	51	9	33
		Last call	62	169	33	109	24	77	15	51
65	TCON	Establish connection								
		First call	85	207	54	131	34	83	21	49
		Intermediate call	30	138	20	78	9	61	6	39
		Last call	30	146	20	100	10	75	7	49

FB No.	FB Name	Description	Execution Time in µs							
			CPU 412-5H solo	CPU 412-5H redundant	CPU 414-5H solo	CPU 414-5H redundant	CPU 416-5H solo	CPU 416-5H redundant	CPU 417-5H solo	CPU 417-5H redundant
66	TDISCON	Terminate connection First call	60	214	33	115	23	102	13	64
		Intermediate call	24	130	20	99	9	61	6	41
		Last call	30	146	21	100	10	75	7	49
67	TUSEND	Send data via UDP (n bytes) First call	101 + n*0.014	239 + n*0.022	62 + n*0.01	159 + n*0.012	41 + n*0.008	107 + n*0.008	26 + n*0.008	69 + n*0.008
		Intermediate call	39	109	23	69	15	52	9	33
		Last call	39	109	23	69	15	52	9	33
68	TURCV	Receive data via UDP First call	78	185	47	109	38	103	19	51
		Intermediate call	39	108	23	69	15	47	9	33
		Last call	83	191	48	121	24	47	23	59

Sublist of the System Status List (SSL)

SSL ID	Information Functions
	Module Identification
0111	One ident. data record only
	CPU Characteristics
0012	CPU features, all features
0112	Features of a group
0F12	Only SSL partial list header information
	User Memory Area
0113	Only partial list header information
	Work memory
	System Areas
0014	System areas, all system areas
0F14	Only partial list header information
	Block Types
0015	Block types, data records for all block types

SSL ID	Information Functions
	Status Module LEDs
0019	Status of all module LEDs
0F19	Only partial list header information
	Component Identification
001C	Identification of all components
011C	Identification of one component
021C	Identification of all components of an H-system CPU
031C	Identification of a component of all redundant CPUs of an H–system
0F1C	Only SSL partial list header information
	Interrupt Status
0222	Data record for specified interrupt
	Assignment between process image partitions and OBs
0025	Assignment betweeen all process image partitions and OBs within the CPU
0125	Assignment between a process image partition and the corresponding OB

SSL ID	Information Functions
	Communication Status Data
0132	Status data for a communication unit
0232	Status data for a communication unit
	H CPU Group Information
0071	Information on the current status of the H system
0F71	Only partial list header information
	Status of the Module LEDs
0174	Status of one LED
	Switched DP Slaves in the H System
0075	Collective information
0C75	Communication status between the H system and a switched DP slave / IO device
0F75	Only SSL partial list header information
	DP Master System Information
0090	Information about all the DP master systems known to the CPU
0190	Information about a DP master system
0F90	Only SSL partial list header information

SSL ID	Information Functions
	Module Status Information (A maximum of 27 data records are supplied)
0591	Module status information of all submodules of the host module
0C91	Status information of a module in the central rack or connected to an integrated DP interface module via the logical base address
4C91	Status information of a module connected to an external DP interface module via the logical base address
0D91	Status information of all modules in the specified rack/in the specified DP station/in the specified PNIO station

SSL ID	Information Functions
	Rack/Station Status Information
0092	Expected status of the central racks/stations of a DP master system
4092	Expected status of the stations of a DP master system which is connected via an external DP interface module
0292	Actual status of the central racks/stations of a DP master system
4292	Actual status of the stations of a DP master system which is connected via an external DP interface module
0392	Status of the back-up battery of a CPU rack if at least one battery fails
0492	Status of the entire back-up batteries of all racks of the a CPU
0592	Actual status of the racks in the central configuration/stations of DP master system which is connected via an external DP interface module.
0692	OK status of the expansion units in the central configuration/stations of a DP master system which is connected via an integrated DP interface module.
4692	OK status of the stations of a DP master system which is connected via an external DP interface module.
	Rack /Station Status Information
0094	Expected status of central rack, stations of a DP station at an integrated interface, stations of an IO controller system at an integrated interface
0294	Actual status of central rack, stations of DP station at an integrated interface, stations of an IO controller system at an integrated interface
0694	Diagnostic status of central rack, stations of a DP station at an integrated interface, stations of an IO controller system at an integrated interface
0794	Maintenance status Wartungszustand of central rack, stations of a DP station at an integrated interface, stations of an IO controller system at an integrated interface
0F94	Only SSL partial list header information

SSL ID	Information Functions
	Extended DP master system- / PROFINET IO system information
0195	Extended information on a DP master system / PROFINET IO system
0F95	Only SSL partial list header information
	Rack status information of all submodules of a specified module
0696	with PROFINET IO at an integrated interface
0C96	Module status information on a central module/submodule, at an integrated PROFIBUS DP interface or at an integrated PROFINET interface
	Diagnostic buffer (up to 21 data records are supplied)
00A0	All entries that can be delivered in the current operating mode
01A0	The latest entries with the number specified by the index
0FA0	Only SSL partial list header information
	Module diagnostic data
00B1	The first four diagnostic bytes of a module (DS0)
00B2	All diagnostic data of a module (< 220 bytes, DS1) (no DP module)
00B3	All diagnostic data of a module (< 220 bytes, DS1)
00B4	Diagnostic data of a DP slave

Index of Instructions