Block diagram

Memories (P. 017-024)

018 - Level shifters
019 - Level shifters
020 - SDRAM - Micron
021 - SDRAM - ISSI
022 - Burst mode FLASH
023 - EMC connectors

Test and Debug (P. 002-008)

002 - LEDs
003 - User GPIOs, octal switch
004 - Debug bus switch, TMP, EEPROM, RS485
005 - Trace MICTOR
006 - Trace, User GPIOs bus switches
007 - USB
008 - Use Case MICTORs

ERTEC 200P (P. 009-014)

009 - ERTEC 200P
010 - ERTEC 200P
011 - ERTEC 200P
012 - ERTEC 200P
013 - ERTEC 200P - PWR
014 - ERTEC 200P - PWR

RJ45, POF (P. 015-016)

015 - RJ45
016 - POF
017 - POF

FPGA (P. 025-027)

024 - FPGA
025 - FPGA
026 - FPGA

PSU (P. 029-032)

028 - External PSU convertor
029 - Power convertors
030 - Power switching
031 - Power sensing

PCIe (P. 028)

027 - PCIe connector

RST, CFG (P. 033-034)

032 - Config pin headers
033 - Reset circuit

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Ind.	Rev.	Modification	Date	Name
	002			

Date	14.1.2013
Init.	
Appr.	
Norm	

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EB200P
Documentation
Block Diagram
Circuit Diagram

Item No.:

A5E31374985A

Sheet 1
40 Sheets

User and status LEDs

FPGA_INITN
FPGA_DONE
FPGA_INFO
PSU_PG
GPIO[0-95]
USER_GPIO[0-15]

FPGA_INITN
FPGA_DONE
FPGA_INFO
PSU_PG

User LEDs

D2 74ALVC16244

		PCB
USER_GPIO[0]	R2 750R, H20 LOL29K ORANGE, H21 LOL29K ORANGE	User GPIO 0
USER_GPIO[1]	R3 750R, H22 LOL29K ORANGE	User GPIO 1
USER_GPIO[2]	R4 750R, H23 LOL29K ORANGE	User GPIO 2
USER_GPIO[3]	R5 750R, H24 LOL29K ORANGE	User GPIO 3
USER_GPIO[4]	R6 750R, H25 LOL29K ORANGE	User GPIO 4
USER_GPIO[5]	R7 750R, H26 LOL29K ORANGE	User GPIO 5
USER_GPIO[6]	R1 750R, H27 LOL29K ORANGE	User GPIO 6
USER_GPIO[7]	R8 750R, H28 LOL29K ORANGE	User GPIO 7
USER_GPIO[8]	R9 750R, H29 LOL29K ORANGE	User GPIO 8
USER_GPIO[9]	R10 750R, H30 LOL29K ORANGE	User GPIO 9
USER_GPIO[10]	R11 750R, H31 LOL29K ORANGE	User GPIO 10
USER_GPIO[11]	R12 750R, H32 LOL29K ORANGE	User GPIO 11
USER_GPIO[12]	R13 750R, H33 LOL29K ORANGE	User GPIO 12
USER_GPIO[13]	R14 750R, H34 LOL29K ORANGE	User GPIO 13
USER_GPIO[14]	R15 750R, H35 LOL29K ORANGE	User GPIO 14
USER_GPIO[15]	R16 750R	User GPIO 15

GND

C1 2u2 16 V, C2 2u2 16 V, C3 100n 16 V, C4 100n 16 V — P3.3V / GND

D2 — max 40mA — P3.3V — VCC (42, 31, 18, 7) — GND (4, 10, 15, 21, 28, 34, 39, 45)

D3 — max 40mA — P3.3V — VCC (42, 31, 18, 7) — GND (4, 10, 15, 21, 28, 34, 39, 45)

GPIO[0-95]

D3 74ALVC16244

GPIO[25]
GPIO[26]
GPIO[27]
GPIO[28]
GPIO[29]
GPIO[30]
GPIO[31]

D3 74ALVC16244

GND

FPGA LEDs

R17 750R, H6 LSL29K RED	P3.3V	FPGA INIT (ERROR)
R18 750R, H5 LGL29K GREEN		FPGA DONE
R398 750R, H36 LOL29K ORANGE		FPGA INFO

Status LEDs

R19 750R, H4 LGA67K GREEN	Bracket Sync
R20 750R, H3 LGA67K GREEN	Bracket Power
R21 750R, H2 LYA67K YELLOW	Bracket Maintenance
R22 750R, H1 LSA67K RED	Bracket Error
R23 750R, H10 LGL29K GREEN	PCB Power
R24 750R, H11 LSL29K RED	PCB Error
R25 750R, H12 LYL29K YELLOW	PCB Maintenance
R26 750R, H13 LYL29K YELLOW	PCB Diagnostic
R27 750R, H14 LGL29K GREEN	PCB PROFIenergy
R28 750R, H15 LGL29K GREEN	PCB Sync
R29 750R, H16 LYL29K YELLOW	PCB FO-1
R30 750R, H17 LYL29K YELLOW	PCB FO-2

GND

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Init.	
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Norm	

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EB200P
Test and debug
LEDs
Circuit Diagram

Item No.:

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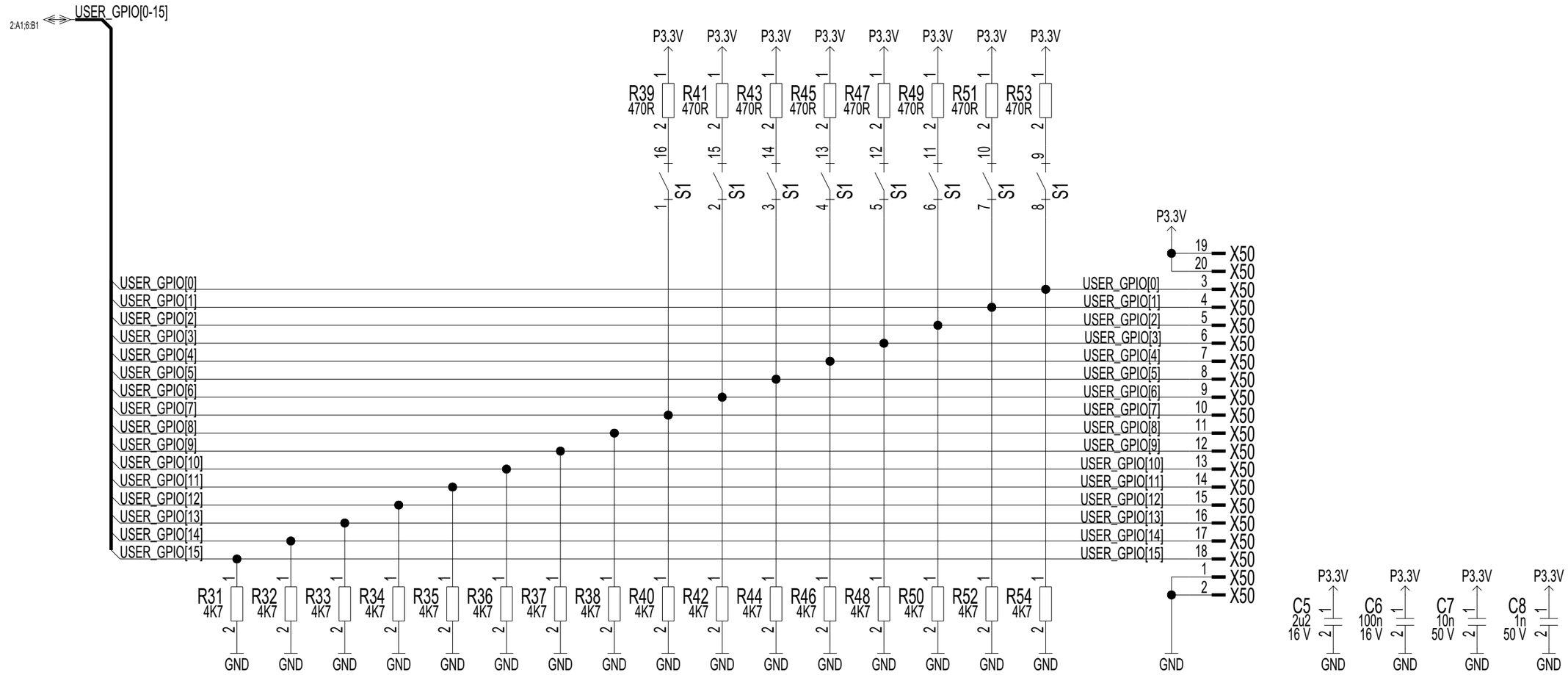
Sheet 2
40 Sheets

User GPIOs



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	002			

Date	14.1.2013
Init.	
Appr.	
Norm	

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EB200P
Test and debug
User octal switch and GPIOs
Circuit Diagram

Item No.:

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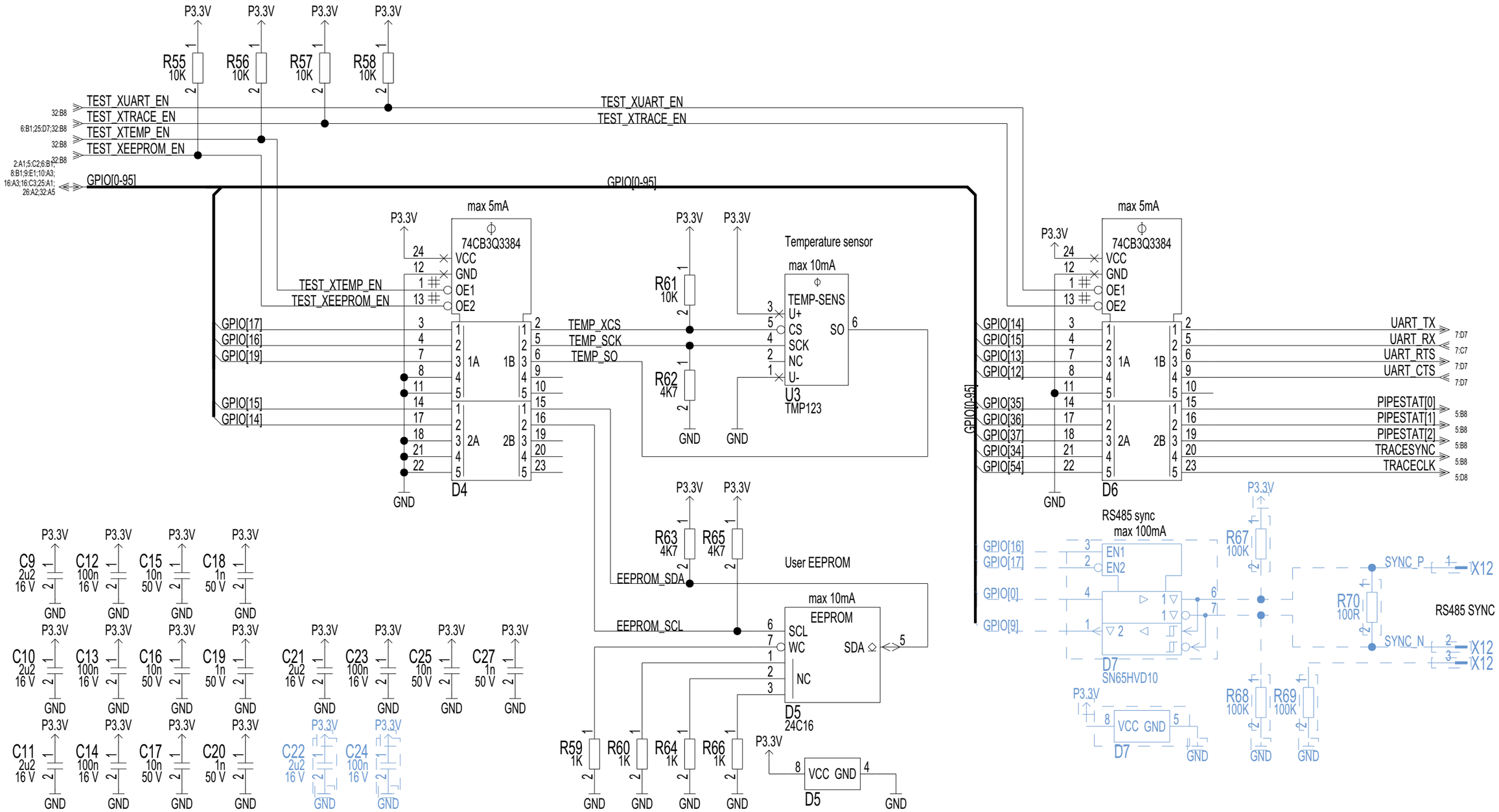
Sheet 3
40 Sheets



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EB200P
Test and debug
Debug bus switch, TMP, EEPROM, RS485
Circuit Diagram

Item No.:

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Sheet 4
40 Sheets

Trace and JTAG conectors

ERTEC 200P JTAG connector

TRACE_DBACK
TRACE_DBGRQ
ERTEC_XSRST
ERTEC_TDO
ERTEC_RTCK
ERTEC_TCK
ERTEC_TMS
ERTEC_TDI
ERTEC_XTRST

P3.3V
X31 1
X31 3
X31 5
X31 7
X31 9
X31 11
X31 13
X31 15
X31 17 JTAG_DBGRQ
X31 19 JTAG_DBACK

P3.3V
X31 2
X31 4
X31 6
X31 8
X31 10
X31 12
X31 14
X31 16
X31 18
X31 20
GND

GPIO[0-95]
GPIO[3] — R71 0R — GPIO[2]
GPIO[2] — R72 0R

R406 10K
GND

ERTEC 200P trace connector

X30 37 TRACEPKT[8]
X30 35 TRACEPKT[9]
X30 33 TRACEPKT[10]
X30 31 TRACEPKT[11]
X30 29 TRACEPKT[12]
X30 27 TRACEPKT[13]
X30 25 TRACEPKT[14]
X30 23 TRACEPKT[15]
X30 21 ERTEC_XTRST
X30 19 ERTEC_TDI
X30 17 ERTEC_TMS
X30 15 ERTEC_TCK
X30 13 ERTEC_RTCK
X30 11 ERTEC_TDO
X30 9 ERTEC_XSRST
X30 7 TRACE_DBGRQ
X30 5
X30 3
X30 1

R407 10K
GND

TRACEPKT[0-15] → TRACEPKT[0-15] 6:B8
X30 38 PIPESTAT[0]
X30 36 PIPESTAT[1]
X30 34 PIPESTAT[2]
PIPESTAT[0-2] 4:C8
X30 32 TRACESYNC
TRACESYNC 4:D8
X30 30 TRACEPKT[0]
X30 28 TRACEPKT[1]
X30 26 TRACEPKT[2]
X30 24 TRACEPKT[3]
X30 22 TRACEPKT[4]
X30 20 TRACEPKT[5]
X30 18 TRACEPKT[6]
X30 16 TRACEPKT[7]

P3.3V
X30 14
X30 12
X30 10
X30 8 TRACE_DBACK
X30 6 TRACECLK
TRACECLK 4:D8
X30 4
X30 2

FPGA JTAG connector

P3.3V — C29 2u2 16 V — GND
P3.3V — C30 100n 16 V — GND
P3.3V — C31 10n 50 V — GND
P3.3V — C32 1n 50 V — GND

P3.3V
X32 1
X32 3
X32 5
X32 7
X32 9
FPGA_DONE 2:A1;25:B6
FPGA_TDO 24:B1
FPGA_TDI 24:B1
FPGA_TMS 24:B1
FPGA_TCK 24:B1
FPGA_PROGRAMN 25:B6

P3.3V
X32 2
X32 4
X32 6
X32 8
X32 10
GND

X30 S1
X30 S2
X30 S3
X30 S4
X30 S5
GND

P3.3V — C33 2u2 16 V — GND
P3.3V — C35 100n 16 V — GND
P3.3V — C37 10n 50 V — GND
P3.3V — C39 1n 50 V — GND
P3.3V — C34 2u2 16 V — GND
P3.3V — C36 100n 16 V — GND
P3.3V — C38 10n 50 V — GND
P3.3V — C40 1n 50 V — GND

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EB200P
Debug
Trace Mictor, FPGA JTAG, ERTEC JTAG
Circuit Diagram

Item No.:

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Sheet 5
40 Sheets

Bus swithches for user GPIOs and trace interface

P3.3V

R73
10K

TEST_XUSERGPIO_EN
TEST_XTRACE_EN
GPIO[0-95]
USER_GPIO[0-15]

32:B8
4:B1;25:D7;32:B8
2:A1;4:B1;5:C2;
8:B1;9:E1;10:A3;
16:A3;16:C3;25:A1;
26:A2;32:A5
2:A1;3:B2

Bus swithches for user GPIOs

Bus swithches for trace interface

TRACEPKT[0-15]
5:B8

max 5mA
74CB3Q3384
VCC
GND
OE1
OE2
1A
1B
2A
2B

D8: GPIO[0] GPIO[1] GPIO[2] GPIO[3] GPIO[4] GPIO[5] GPIO[6] GPIO[7] GPIO[16] GPIO[17] → USER_GPIO[0] USER_GPIO[1] USER_GPIO[2] USER_GPIO[3] USER_GPIO[4] USER_GPIO[5] USER_GPIO[6] USER_GPIO[7] USER_GPIO[8] USER_GPIO[9]

D9: GPIO[18] GPIO[19] GPIO[20] GPIO[21] GPIO[22] GPIO[23] → USER_GPIO[10] USER_GPIO[11] USER_GPIO[12] USER_GPIO[13] USER_GPIO[14] USER_GPIO[15]

D10: GPIO[38] GPIO[39] GPIO[40] GPIO[41] GPIO[42] GPIO[43] GPIO[44] GPIO[45] GPIO[46] GPIO[47] → TRACEPKT[0] TRACEPKT[1] TRACEPKT[2] TRACEPKT[3] TRACEPKT[4] TRACEPKT[5] TRACEPKT[6] TRACEPKT[7] TRACEPKT[8] TRACEPKT[9]

D11: GPIO[48] GPIO[49] GPIO[50] GPIO[51] GPIO[52] GPIO[53] GPIO[3] GPIO[2] → TRACEPKT[10] TRACEPKT[11] TRACEPKT[12] TRACEPKT[13] TRACEPKT[14] TRACEPKT[15] TRACE_DBACK TRACE_DBGRQ

TRACE_DBACK 5:A2
TRACE_DBGRQ 5:A2

C41 2u2 16 V
C42 100n 16 V
C43 10n 50 V
C44 1n 50 V
C45 2u2 16 V
C46 100n 16 V
C47 10n 50 V
C48 1n 50 V
C49 2u2 16 V
C50 100n 16 V
C51 10n 50 V
C52 1n 50 V
C53 2u2 16 V
C54 100n 16 V
C55 10n 50 V
C56 1n 50 V

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EB200P
Test and debug
Trace and user GPIOs bus switches
Circuit Diagram

Item No.:

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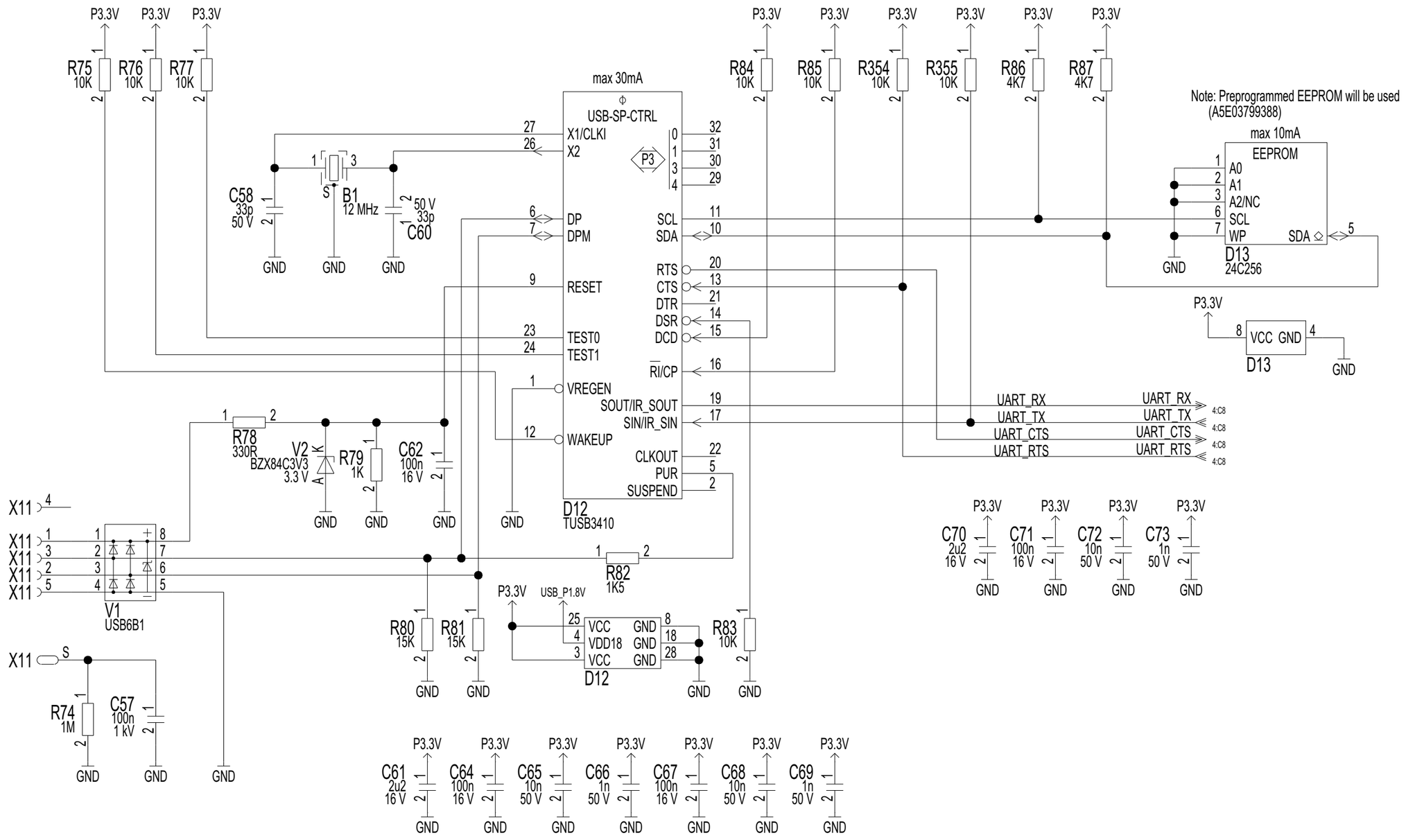
Sheet 6
40 Sheets



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					Norm	

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EB200P
Test and debug
Serial over USB
Circuit Diagram

Item No.:

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Sheet 7
40 Sheets

Use case connectors

P3.3V
R366 1K
PM_FLASH_XRESET
33:C7
ERTEC_REF_CLK
GPIO[0-95]
2:A1;4:B1;8:C2;
6:B1;9:E1;10:A3;
16:A3;16:C3;25:A1;
26:A2;32:A5

Use case 0

X20	37	GPIO[16]	X20	38	GPIO[0]		
X20	35	GPIO[17]	X20	36	GPIO[1]		
X20	33	GPIO[18]	X20	34	GPIO[2]		
X20	31	GPIO[19]	X20	32	GPIO[3]		
X20	29	GPIO[20]	X20	30	GPIO[4]		
X20	27	GPIO[21]	X20	28	GPIO[5]		
X20	25	GPIO[22]	X20	26	GPIO[6]		
X20	23	GPIO[23]	X20	24	GPIO[7]		
X20	21	GPIO[24]	X20	22	GPIO[8]		
X20	19	GPIO[25]	X20	20	GPIO[9]		
X20	17	GPIO[26]	X20	18	GPIO[10]		
X20	15	GPIO[27]	X20	16	GPIO[11]		
X20	13	GPIO[28]	X20	14	GPIO[12]		
X20	11	GPIO[29]	X20	12	GPIO[13]		
X20	9	GPIO[30]	X20	10	GPIO[14]		
X20	7	GPIO[31]	X20	8	GPIO[15]		
X20	5	PM_FLASH_XRESET	X20	6			
X20	3	P3.3V	X20	4	P5.0V		
X20	1		X20	2			

X20: S1, S2, S3, S4, S5 → GND

C74	2u2	16 V	C76	100n	16 V	C78	10n 50 V	C80	1n 50 V
C75	2u2	16 V	C77	100n	16 V	C79	10n 50 V	C81	1n 50 V

Use case 1

X21	37	GPIO[48]	X21	38	GPIO[32]		
X21	35	GPIO[49]	X21	36	GPIO[33]		
X21	33	GPIO[50]	X21	34	GPIO[34]		
X21	31	GPIO[51]	X21	32	GPIO[35]		
X21	29	GPIO[52]	X21	30	GPIO[36]		
X21	27	GPIO[53]	X21	28	GPIO[37]		
X21	25	GPIO[54]	X21	26	GPIO[38]		
X21	23	GPIO[55]	X21	24	GPIO[39]		
X21	21	GPIO[56]	X21	22	GPIO[40]		
X21	19	GPIO[57]	X21	20	GPIO[41]		
X21	17	GPIO[58]	X21	18	GPIO[42]		
X21	15	GPIO[59]	X21	16	GPIO[43]		
X21	13	GPIO[60]	X21	14	GPIO[44]		
X21	11	GPIO[61]	X21	12	GPIO[45]		
X21	9	GPIO[62]	X21	10	GPIO[46]		
X21	7	GPIO[63]	X21	8	GPIO[47]		
X21	5	ERTEC_REF_CLK	X21	6			
X21	3	P3.3V	X21	4	P5.0V		
X21	1		X21	2			

X21: S1, S2, S3, S4, S5 → GND

C82	2u2	16 V	C84	100n	16 V	C86	10n 50 V	C88	1n 50 V
C83	2u2	16 V	C85	100n	16 V	C87	10n 50 V	C89	1n 50 V

Use case 2

X22	37	GPIO[80]	X22	38	GPIO[64]		
X22	35	GPIO[81]	X22	36	GPIO[65]		
X22	33	GPIO[82]	X22	34	GPIO[66]		
X22	31	GPIO[83]	X22	32	GPIO[67]		
X22	29	GPIO[84]	X22	30	GPIO[68]		
X22	27	GPIO[85]	X22	28	GPIO[69]		
X22	25	GPIO[86]	X22	26	GPIO[70]		
X22	23	GPIO[87]	X22	24	GPIO[71]		
X22	21	GPIO[88]	X22	22	GPIO[72]		
X22	19	GPIO[89]	X22	20	GPIO[73]		
X22	17	GPIO[90]	X22	18	GPIO[74]		
X22	15	GPIO[91]	X22	16	GPIO[75]		
X22	13	GPIO[92]	X22	14	GPIO[76]		
X22	11	GPIO[93]	X22	12	GPIO[77]		
X22	9	GPIO[94]	X22	10	GPIO[78]		
X22	7	GPIO[95]	X22	8	GPIO[79]		
X22	5		X22	6			
X22	3	P3.3V	X22	4	P5.0V		
X22	1		X22	2			

X22: S1, S2, S3, S4, S5 → GND

C90	2u2	16 V	C92	100n	16 V	C94	10n 50 V	C96	1n 50 V
C91	2u2	16 V	C93	100n	16 V	C95	10n 50 V	C97	1n 50 V

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EB200P
Interfaces
Use case MICTORs
Circuit Diagram

Item No.:

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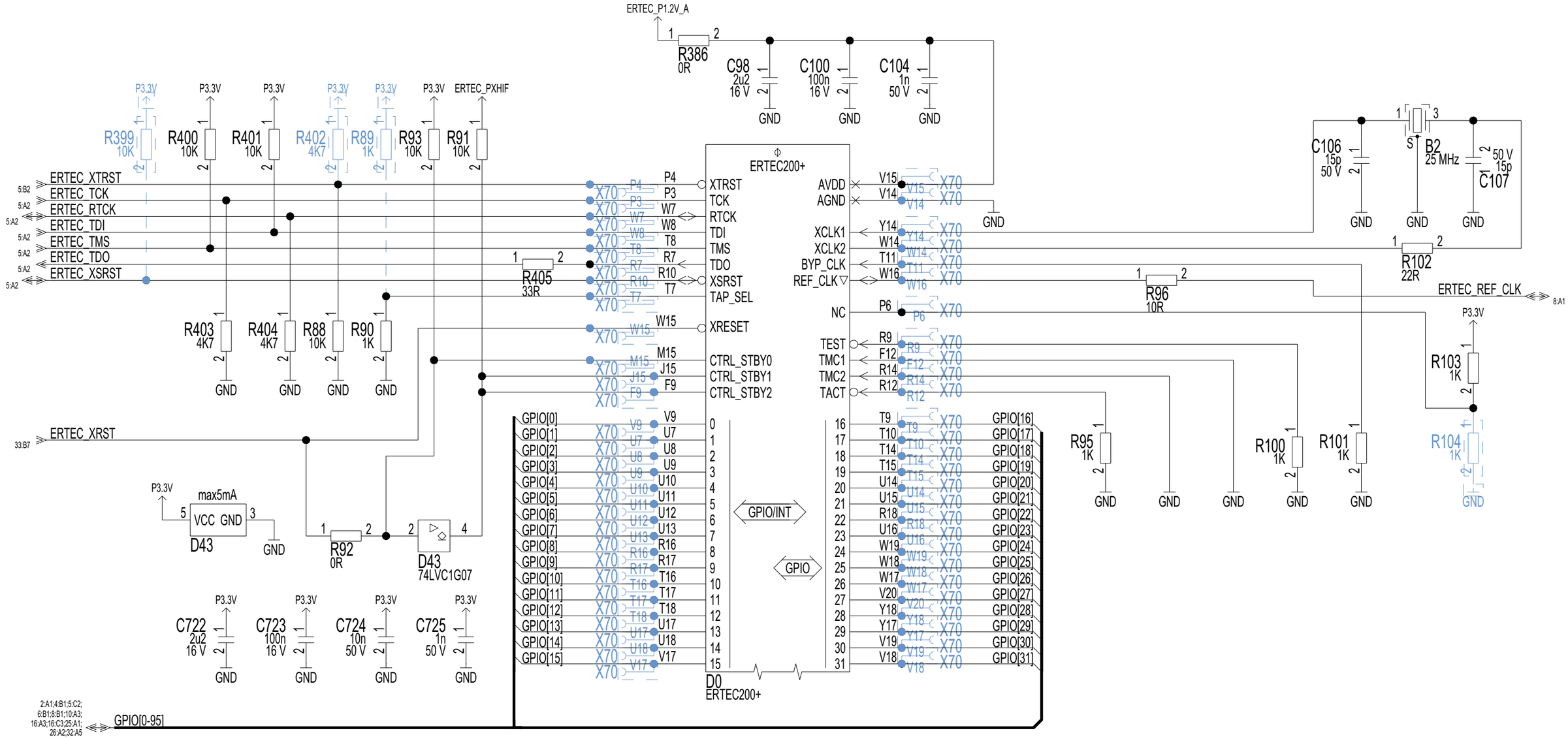
Sheet 8
40 Sheets



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EB200P
ERTEC 200P
ERTEC 200P
Circuit Diagram

Item No.:

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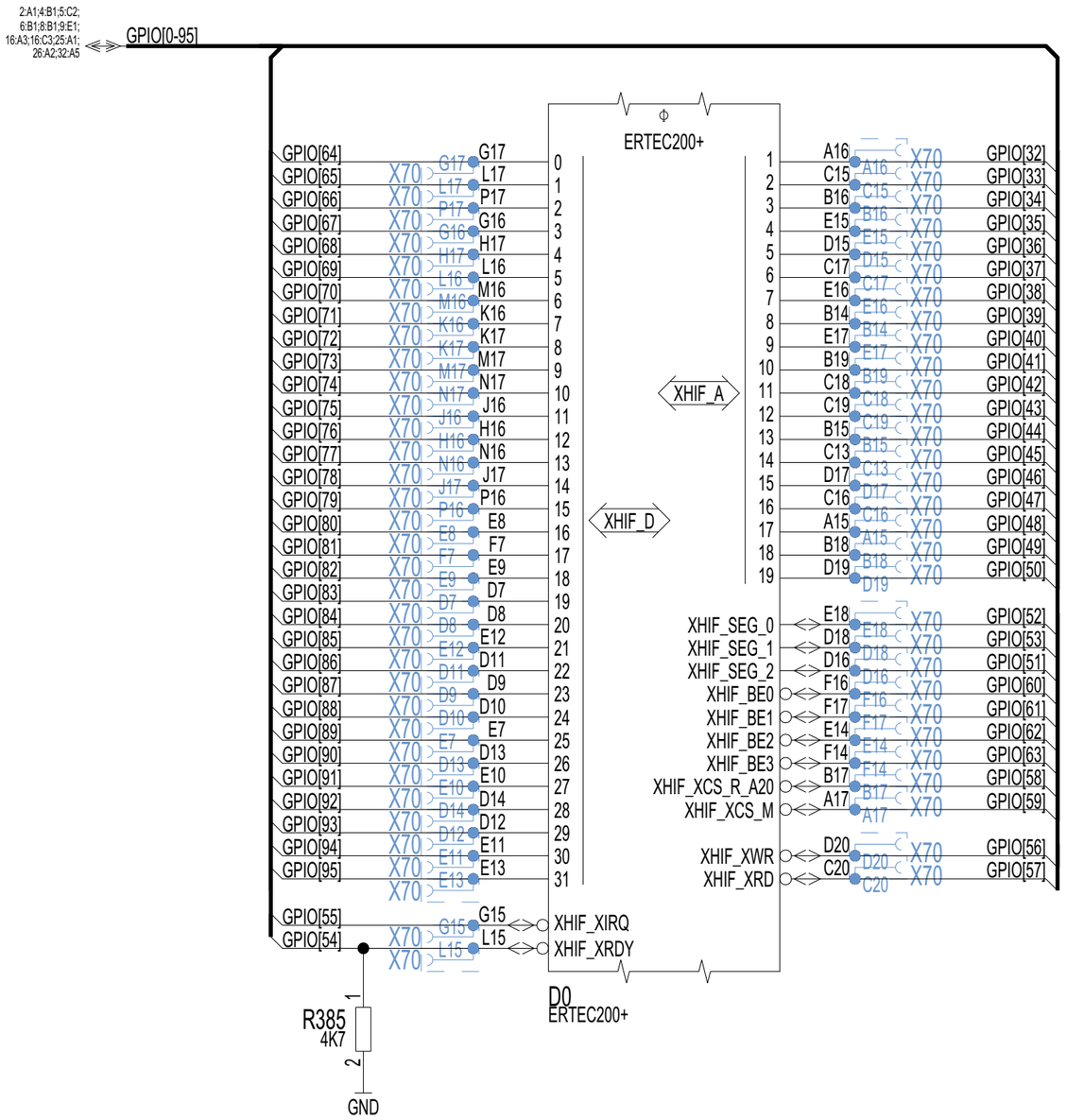
Sheet 9
40 Sheets



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					Appr.	
					Norm	

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EB200P
ERTEC 200P
ERTEC 200P
Circuit Diagram

Item No.:

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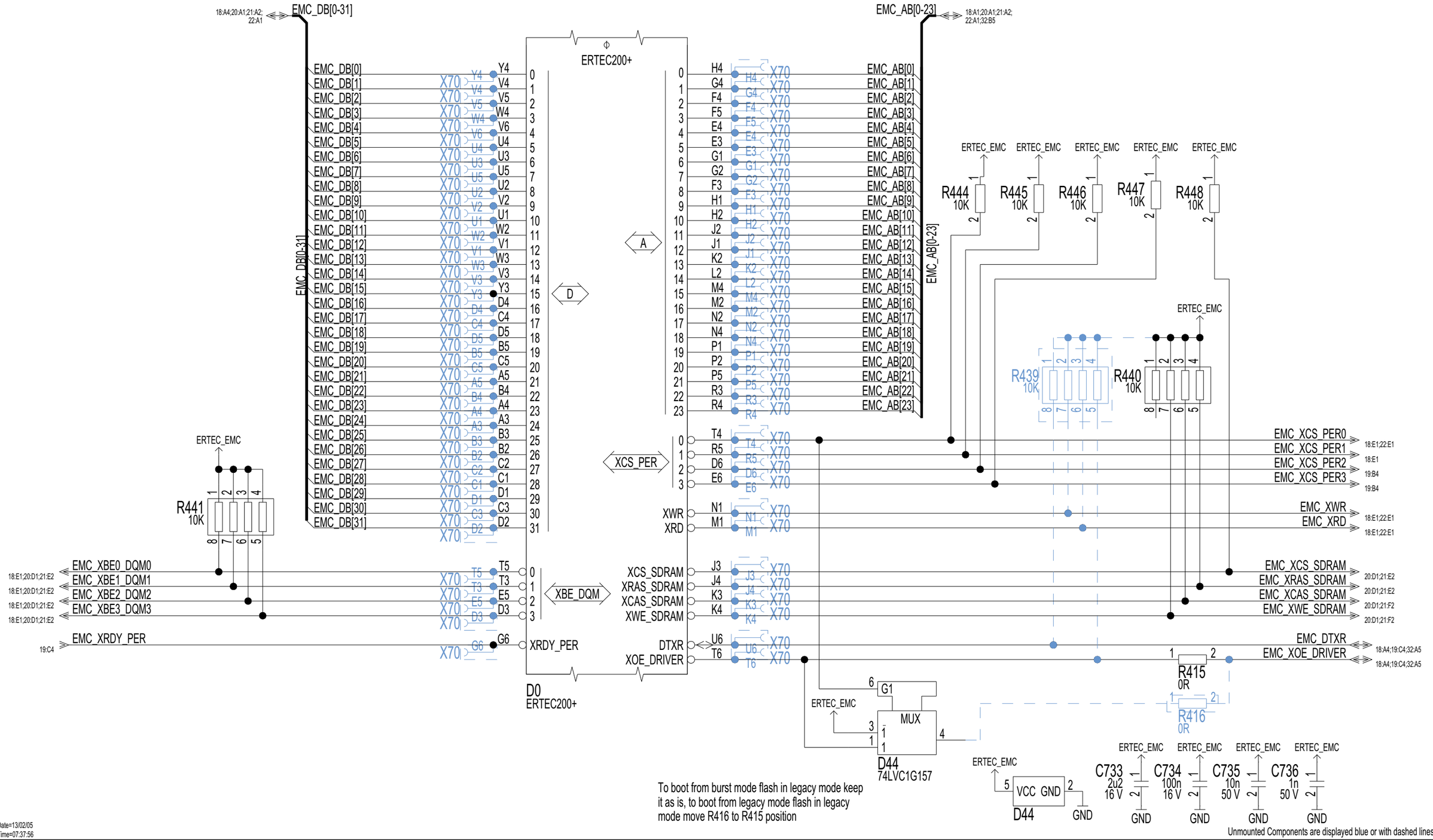
Sheet 10
40 Sheets



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					Appr.	
					Norm	

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EB200P
ERTEC 200P
ERTEC 200P
Circuit Diagram

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Sheet 11
40 Sheets

ERTEC 200P - Profinet ports

P1.5V_A_SEP
ERTEC_P3.3V_A
P3.3V
ERTEC_P1.5V_A

R394 0R
R397 0R
R393 0R

C132 2u2 16 V
C133 100n 16 V
C134 10n 50 V
C137 1n 50 V
C108 2u2 16 V
C112 100n 16 V
C116 10n 50 V
C120 1n 50 V
C124 2u2 16 V
C125 100n 16 V
C126 10n 50 V
C127 1n 50 V
C128 2u2 16 V
C129 100n 16 V
C130 10n 50 V
C131 1n 50 V
C111 2u2 16 V
C115 100n 16 V
C119 10n 50 V
C123 1n 50 V
C109 2u2 16 V
C113 100n 16 V
C117 10n 50 V
C121 1n 50 V
C110 2u2 16 V
C114 100n 16 V
C118 10n 50 V
C122 1n 50 V
C135 2u2 16 V
C138 100n 16 V
C141 10n 50 V
C144 1n 50 V
C136 2u2 16 V
C139 100n 16 V
C142 10n 50 V
C145 1n 50 V
GND

ERTEC200+

L19	VSSAPLLCB	ATP	K18
L20	VDDACB	VDD33ESD	G18
K20	VDDAPLL		
F20	DVDD1	DGND1	F19
R20	DVDD3	DGND3	R19
B10	VDD_PECL1		
W10	VDD_PECL2		
		EXTRES	K19
G20	P1VDDARXTX	P2VDDARXTX	P20
H18	PVSSA	PVSSA	N18
J18	PVSSA	PVSSA	M18
B11	P1SDXP	P2SDXP	W11
A11	P1SDXN	P2SDXN	Y11
B9	P1TDXP	P2TDXP	W9
A9	P1TDXN	P2TDXN	Y9
B12	P1RDXP	P2RDXP	W12
A12	P1RDXN	P2RDXN	Y12
J19	P1TXP	P2TXP	M19
J20	P1TXN	P2TXN	M20
H19	P1RXP	P2RXP	N19
H20	P1RXN	P2RXN	N20
C9	P1FXEN	P2FXEN	Y8
T13	A_PHY1	TESTOUT5	B8
T12	A_PHY2	TESTOUT6	A8
U20	L_PHY1	TESTOUT7	V10
U19	L_PHY2	CLK_O_SDRAM0	H5
		CLK_O_SDRAM1	J5
G5	CLK_I_SDRAM	CLK_O_SDRAM2	J6
L5	CLK_I_BF		
K5	XAV_BF	CLK_O_BF0	M5
L4	XRDY_BF	CLK_O_BF1	N5
		CLK_O_BF2	M6

P1
R124 12K4
R122 0R
R123 0R

P1_SDXP 17:C3
P1_SDXN 17:C3
P1_TDXP 16:E1
P1_TDXN 16:E1
P1_RDXP 16:E1
P1_RDXN 16:E1
P1_TXP 15:C1
P1_TXN 15:C1
P1_RXP 15:C1
P1_RXN 15:C1
P1_FXEN 16:E1
P1_ACT 15:C1;17:F3
P2_ACT 15:E1;17:E3
P1_LINK 15:C1;17:E3
P2_LINK 15:E1;17:E3
EMC_XRDY_BF 22:E1

P2_SDXP 17:B3
P2_SDXN 17:B3
P2_TDXP 16:B1
P2_TDXN 16:B1
P2_RDXP 16:B1
P2_RDXN 16:C1
P2_TXP 15:E1
P2_TXN 15:E1
P2_RXP 15:E1
P2_RXN 15:E1
P2_FXEN 16:B1
EMC_CLK_O_SDRAM1 20:D1;21:E2
EMC_CLK_O_SDRAM2 20:D1;21:E2
EMC_CLK_O_BF1 22:E1
EMC_CLK_O_BF2 22:E1

ERTEC_EMC
R125 10K
R127 10K
C140 15p 50 V
C143 15p 50 V
R126 49R9
R128 49R9
R436 10K
EMC_XAV_BF 22:E1

D0
ERTEC200+

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Date 14.1.2013
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EB200P
ERTEC 200P
ERTEC 200P
Circuit Diagram

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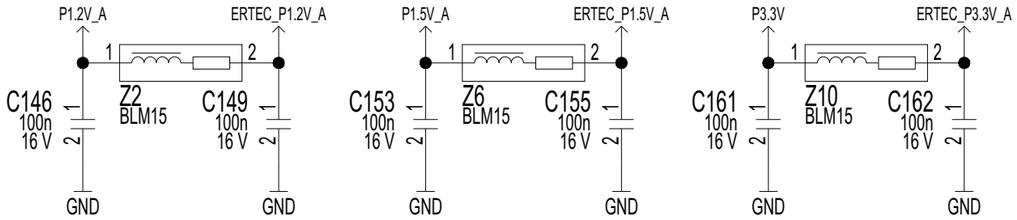
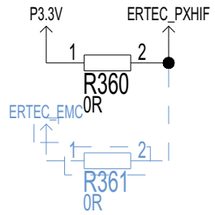
A5E31374985A

Sheet 12
40 Sheets

ERTEC 200P - power supply pins





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EB200P
Power supply
ERTEC 200P
Circuit Diagram

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Sheet 13
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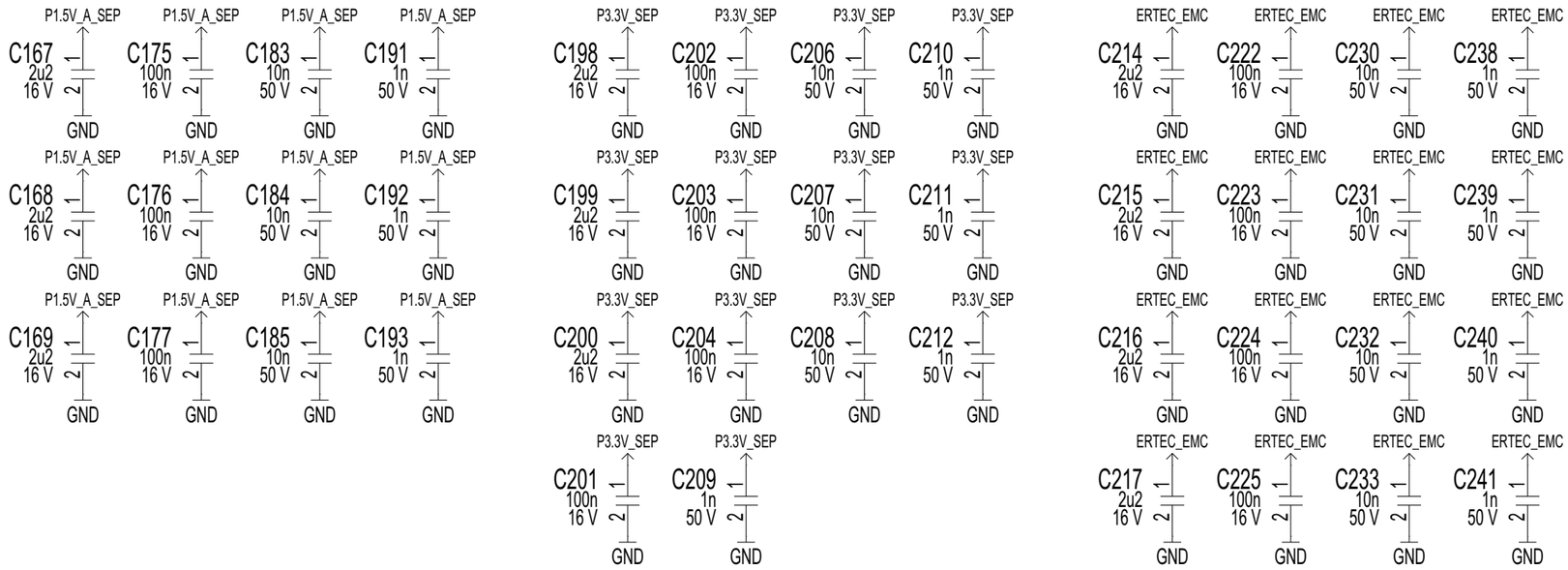
ERTEC 200P - power supply capacitors



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EB200P
Power supply
ERTEC 200P capacitors
Circuit Diagram

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40 Sheets

TAP

Profinet ports

Place R129, R130, R133, R134
R135, R136, R139, R140 close to
Ertec

P5.0V — Z12 BLM15 — ERTEC_P5.0V_A
C245 100n 16 V, C248 100n 16 V, C707 10u 10 V — GND
R131 10K, R132 10K, R137 10K, R138 10K
C251 100n 16 V, C252 100n 16 V
max 50mA
N1 AD8131, N2 AD8131 (U+, U-, VOCM)
R147 49R9, R148 49R9, R149 49R9, R150 49R9
TAPA_P, TAPA_N, TAPB_P, TAPB_N

P3.3V — Z13 BLM15
C246 100n 16 V, C249 100n 16 V, C708 10u 10 V
R129 49R9, R133 49R9, R135 49R9, R139 49R9
P1_TXP, P1_TXN, P1_RXP, P1_RXN (12:D3)
P1_LINK, P1_ACT (12:E3;17:E3, 12:D3;17:F3)

P3.3V — Z14 BLM15
C247 100n 16 V, C250 100n 16 V, C709 10u 10 V
R130 49R9, R134 49R9, R136 49R9, R140 49R9
P2_TXP, P2_TXN, P2_RXP, P2_RXN (12:D7)
P2_LINK, P2_ACT (12:E3;17:E3)

C253 10n 50 V, C255 10n 50 V
C254 10n 50 V, C256 10n 50 V

Profinet port 1

R141 10R, R143 10R, R145 470R, R151 470R
A10, A9, A1, A2, A3, A4, A5, A6, A7, A8, A12, A11
S, S1, X1 RJ45

Profinet port 2

R142 10R, R144 10R, R146 470R, R152 470R
B10, B9, B1, B2, B3, B4, B5, B6, B7, B8, B12, B11
S2, X1 RJ45

TAP A - Profinet port 1 Tx

ERTEC_P5.0V_A
R153 1K, R157 1K, R154 1K, R158 1K
C263 10n 50 V, C265 10n 50 V
R161 100R
C10, C9, C1, C2, C3, C4, C5, C6, C7, C8, C12, C11
S3, X1 RJ45

TAP A - Profinet port 1 Rx

ERTEC_P5.0V_A
R155 1K, R159 1K, R156 1K, R160 1K
C264 10n 50 V, C266 10n 50 V
R162 100R
D10, D9, D1, D2, D3, D4, D5, D6, D7, D8, D12, D11
S4, X1 RJ45

C731 4n7 1kV, C732 4n7 1kV
R163 1M, R164 1M
EARTH

C257 2u2 16 V, C259 100n 16 V, C261 10n 50 V, C267 1n 50 V
C258 2u2 16 V, C260 100n 16 V, C262 10n 50 V, C268 1n 50 V

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EB200P
Interfaces
ERTEC 200P ethernet ports - RJ45
Circuit Diagram

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Sheet 15
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POFs

P3.3V
L1 10 uH
L2 10 uH
C270 10u 10 V
C272 10u 10 V
GND

2:A1;4:B1;5:C2; 6:B1;8:B1;9:E1; 10:A3;16:C3;25:A1; 26:A2;32:A5
GPIO[0-95]
GPIO[7]
GPIO[6]

POF port 2

R169 130R
R173 130R
R193 4K7
R195 0R
R197 0R
R201 4K7

max 300mA

TRANSCEIVER
7 VCCTX
8 VEETX
10 TD+
11 TD-
9 TX_DISABLE
12 SCL
1 SDA
VCCRX 3
VEERX 2
RD+ 6
RD- 5
SD 4
X3
QFBR-5978

P2_SD 17:B6

C274 10u 10 V
C278 100n 16 V
C282 10n 50 V
C286 1n 50 V
C275 10u 10 V
C279 100n 16 V
C283 10n 50 V
C287 1n 50 V

Tx termination in Transciever included

R165 150R
R166 150R
P2_TDXP 12:C7
P2_TDXN 12:C7
P2_FXEN 12:D7
P2_RDXP 12:D7
P2_RDXN 12:D7

R170 0R
R174 0R
R199 1K

Resitor placement:
Close to ERTEC : R165,R166,R170,R174
R169, R173

How to instal POF:
1. Remove Qaud RJ45 connector with magnetics
2. Solder R169, R173, R195, R197
   0 Ohm (A5E00091701)
   130 Ohm (A5E00375218)
3. Solder R171, R175, R196, R198
   0 Ohm (A5E00091701)
   130 Ohm (A5E00375218)
4. Replace R170, R174, with 82 Ohm resistor (A5E00375108)
5. Replace R172, R176, with 82 Ohm resistor (A5E00375108)
6. Solder both POF transceivers (A5E00384758)
7. Be careful with user GPIOs pull downs (R46, R44, R42, R40)

P3.3V
L3 10 uH
L4 10 uH
C271 10u 10 V
C273 10u 10 V
GND

2:A1;4:B1;5:C2; 6:B1;8:B1;9:E1; 10:A3;16:A3;25:A1; 26:A2;32:A5
GPIO[0-95]
GPIO[5]
GPIO[4]

POF port 1

R171 130R
R175 130R
R194 4K7
R196 0R
R198 0R
R202 4K7

max 300mA

TRANSCEIVER
7 VCCTX
8 VEETX
10 TD+
11 TD-
9 TX_DISABLE
12 SCL
1 SDA
VCCRX 3
VEERX 2
RD+ 6
RD- 5
SD 4
X4
QFBR-5978

P1_SD 17:C6

C276 10u 10 V
C280 100n 16 V
C284 10n 50 V
C288 1n 50 V
C277 10u 10 V
C281 100n 16 V
C285 10n 50 V
C289 1n 50 V

Tx termination in Transciever included

R167 150R
R168 150R
P1_TDXP 12:C3
P1_TDXN 12:C3
P1_FXEN 12:D3
P1_RDXP 12:D3
P1_RDXN 12:D3

R172 0R
R176 0R
R200 1K

Resitor placement:
Close to ERTEC : R167,R168,R171,R175
R172, R176

Resitor tolerance:
All resistors with value 82 and 130 Ohm have to be with 1% tolerance

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EB200P
Interfaces
ERTEC 200P ethernet ports - POF
Circuit Diagram

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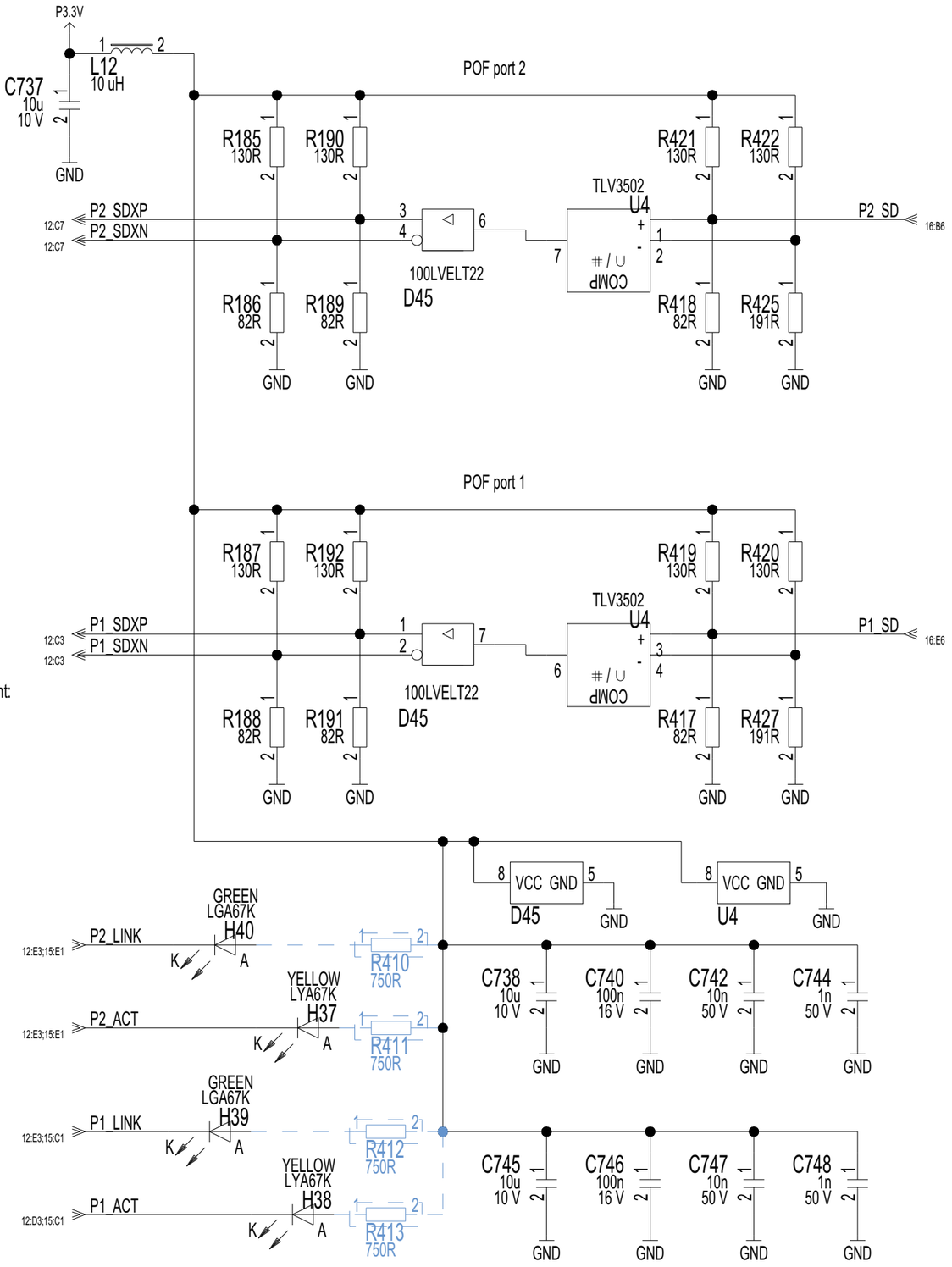

Resitor placement:
Close to ERTEC : R185,R190,R186,R189
R187, R192, R188, R191

Resitor tolerance:
All resistors with value 82 and 130 and 191 Ohm have to be with 1% tolerance

How to instal POF:
1. Solder R410, R411, R412, R413
   750 Ohm (A5E00091712)

Comparator (U4) and PECL (D45) driver placement:
Close to POFs (X3, X4)

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EB200P
Interfaces
ERTEC 200P ethernet ports - POF
Circuit Diagram

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Level shifters

As defualt the level shifter for address bus is disabled. To enable it move R414 to position R203

Level shifters - address bus

ERTEC_EMC ERTEC_EMC

R414 1K R204 1K

EMC_AB[0-23] ← 11:A6;20:A1;21:A2;22:A1;32:B5

LS_AB[0-23] → 23:A2;24:B1;25:A1

D14 74LVC16T245 max 100mA

	48	G3	
	1	3EN1[BA]	
	25	3EN2[AB]	
	24	G6	
		6EN4[BA]	
		6EN5[AB]	
EMC_AB[0]	47	▽1 ◁	2 LS_AB[0]
EMC_AB[1]	46	▷ 2 ▽	3 LS_AB[1]
EMC_AB[2]	44		5 LS_AB[2]
EMC_AB[3]	43		6 LS_AB[3]
EMC_AB[4]	41		8 LS_AB[4]
EMC_AB[5]	40		9 LS_AB[5]
EMC_AB[6]	38		11 LS_AB[6]
EMC_AB[7]	37		12 LS_AB[7]
EMC_AB[8]	36	▽4 ◁	13 LS_AB[8]
EMC_AB[9]	35	▷ 5 ▽	14 LS_AB[9]
EMC_AB[10]	33		16 LS_AB[10]
EMC_AB[11]	32		17 LS_AB[11]
EMC_AB[12]	30		19 LS_AB[12]
EMC_AB[13]	29		20 LS_AB[13]
EMC_AB[14]	27		22 LS_AB[14]
EMC_AB[15]	26		23 LS_AB[15]

D15 74LVC16T245 max 100mA

	48	G3	
	1	3EN1[BA]	
	25	3EN2[AB]	
	24	G6	
		6EN4[BA]	
		6EN5[AB]	
EMC_AB[16]	47	▽1 ◁	2 LS_AB[16]
EMC_AB[17]	46	▷ 2 ▽	3 LS_AB[17]
EMC_AB[18]	44		5 LS_AB[18]
EMC_AB[19]	43		6 LS_AB[19]
EMC_AB[20]	41		8 LS_AB[20]
EMC_AB[21]	40		9 LS_AB[21]
EMC_AB[22]	38		11 LS_AB[22]
EMC_AB[23]	37		12 LS_AB[23]
EMC_XCS_PER0	36	▽4 ◁	13 LS_XCS_PER0 → 23:C6
EMC_XCS_PER1	35	▷ 5 ▽	14 LS_XCS_PER1 → 25:B1
EMC_XWR ← 11:D8	33		16 LS_XWR → 23:C6;24:C1
EMC_XRD ← 11:D8;22:E1	32		17 LS_XRD → 23:C6;24:C1
EMC_XBE0_DQM0 ← 11:D8;22:E1	30		19 LS_XBE0_DQM0 → 23:D3;25:C7
EMC_XBE1_DQM1 ← 11:E1;20:D1;21:E2	29		20 LS_XBE1_DQM1 → 23:D4;26:B6
EMC_XBE2_DQM2 ← 11:E1;20:D1;21:E2	27		22 LS_XBE2_DQM2 → 23:D6;24:B1
EMC_XBE3_DQM3 ← 11:E1;20:D1;21:E2	26		23 LS_XBE3_DQM3 → 23:D7;25:B1

R203 1K

GND

Level shifters - data bus

P3.3V

R205 R207 R209 R211 10K

R206 R208 R210 R212 10K

EMC_DB[0-31] ← 11:A2;20:A1;21:A2;22:A1

LS_DB[0-31] → 23:A2;24:B1;25:A1;26:A2

EMC_XOE_DRIVER ← 11:E8;19:C4;32:A5

EMC_DTXR ← 11:E8;19:C4;32:A5

D16 74LVC16T245 max 100mA

	48	G3	
	1	3EN1[BA]	
	25	3EN2[AB]	
	24	G6	
		6EN4[BA]	
		6EN5[AB]	
EMC_DB[0]	47	▽1 ◁	2 LS_DB[0]
EMC_DB[1]	46	▷ 2 ▽	3 LS_DB[1]
EMC_DB[2]	44		5 LS_DB[2]
EMC_DB[3]	43		6 LS_DB[3]
EMC_DB[4]	41		8 LS_DB[4]
EMC_DB[5]	40		9 LS_DB[5]
EMC_DB[6]	38		11 LS_DB[6]
EMC_DB[7]	37		12 LS_DB[7]
EMC_DB[8]	36	▽4 ◁	13 LS_DB[8]
EMC_DB[9]	35	▷ 5 ▽	14 LS_DB[9]
EMC_DB[10]	33		16 LS_DB[10]
EMC_DB[11]	32		17 LS_DB[11]
EMC_DB[12]	30		19 LS_DB[12]
EMC_DB[13]	29		20 LS_DB[13]
EMC_DB[14]	27		22 LS_DB[14]
EMC_DB[15]	26		23 LS_DB[15]

D17 74LVC16T245 max 100mA

	48	G3	
	1	3EN1[BA]	
	25	3EN2[AB]	
	24	G6	
		6EN4[BA]	
		6EN5[AB]	
EMC_DB[16]	47	▽1 ◁	2 LS_DB[16]
EMC_DB[17]	46	▷ 2 ▽	3 LS_DB[17]
EMC_DB[18]	44		5 LS_DB[18]
EMC_DB[19]	43		6 LS_DB[19]
EMC_DB[20]	41		8 LS_DB[20]
EMC_DB[21]	40		9 LS_DB[21]
EMC_DB[22]	38		11 LS_DB[22]
EMC_DB[23]	37		12 LS_DB[23]
EMC_DB[24]	36	▽4 ◁	13 LS_DB[24]
EMC_DB[25]	35	▷ 5 ▽	14 LS_DB[25]
EMC_DB[26]	33		16 LS_DB[26]
EMC_DB[27]	32		17 LS_DB[27]
EMC_DB[28]	30		19 LS_DB[28]
EMC_DB[29]	29		20 LS_DB[29]
EMC_DB[30]	27		22 LS_DB[30]
EMC_DB[31]	26		23 LS_DB[31]

ERTEC_EMC P3.3V

D14 / D15 / D16 / D17

	42	VCCA	GND 4, 10, 15, 21, 28, 34, 39, 45
	31	VCCA	
	18	VCCB	
	7	VCCB	

GND

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EB200P
Memory
Level shifters
Circuit Diagram

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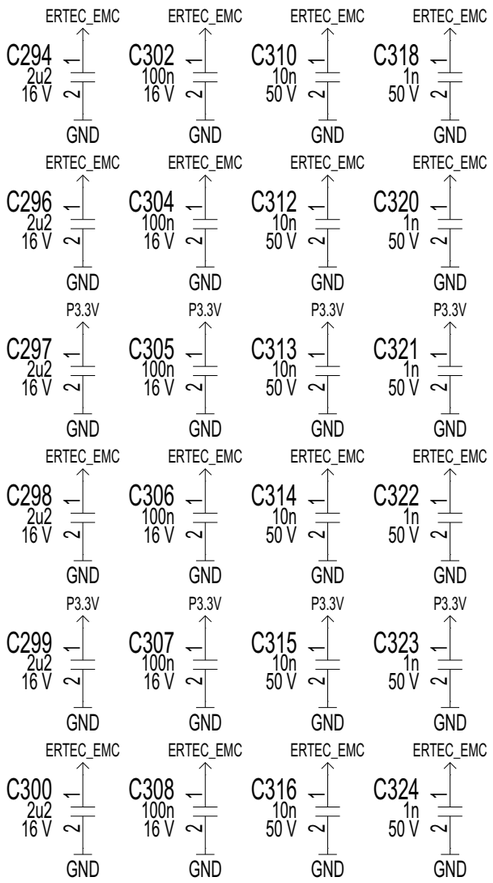
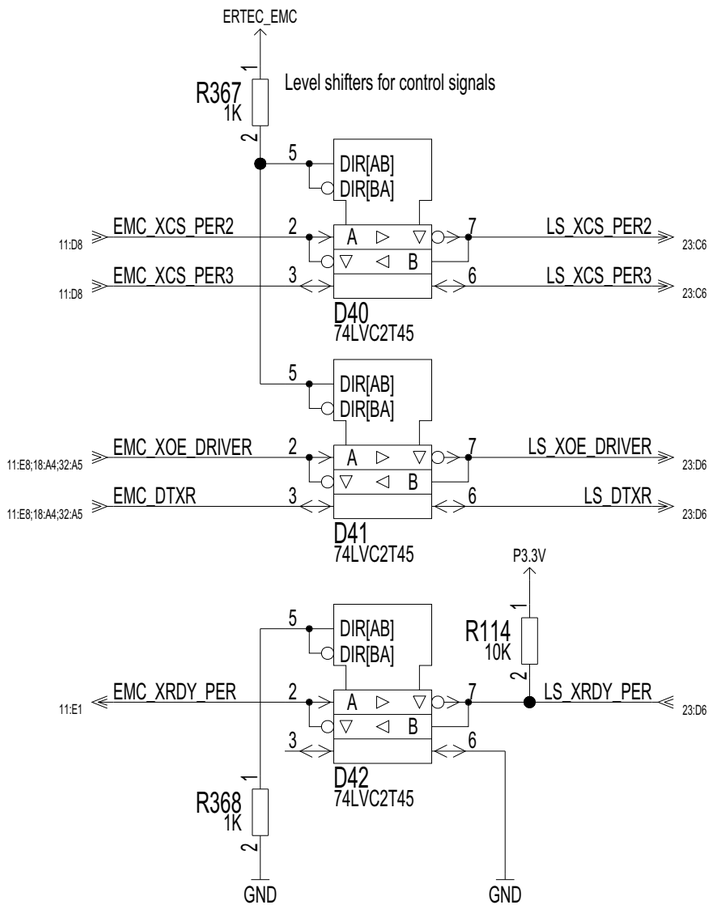
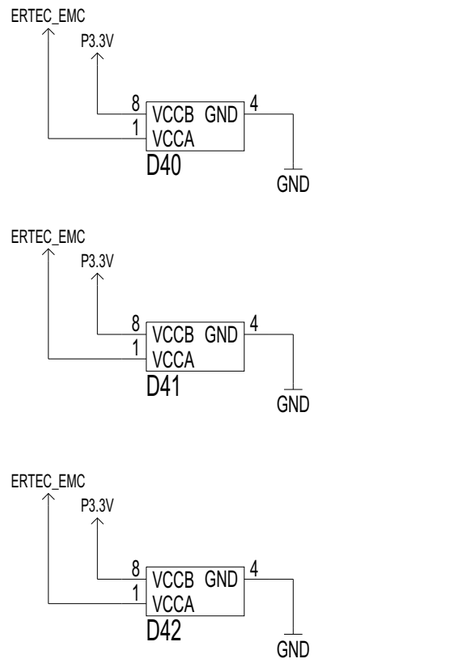
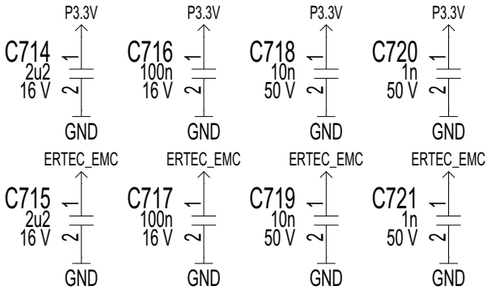
Level shifters, capacitors for level shifters









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11:A2;18:A4;21:A2;22:A1 EMC_DB[0-31]
11:A6;18:A1;21:A2;22:A1;32:B5 EMC_AB[0-23]
22:E1;33:D7 EMC_XRESET
12:E7;21:E2 EMC_CLK_O_SDRAM1
12:E7;21:E2 EMC_CLK_O_SDRAM2
11:E1;18:E1;21:E2 EMC_XBE0_DQM0
11:E1;18:E1;21:E2 EMC_XBE1_DQM1
11:E1;18:E1;21:E2 EMC_XBE2_DQM2
11:E1;18:E1;21:E2 EMC_XBE3_DQM3
11:E8;21:E2 EMC_XCS_SDRAM
11:E8;21:E2 EMC_XRAS_SDRAM
11:E8;21:F2 EMC_XCAS_SDRAM
11:E8;21:F2 EMC_XWE_SDRAM

ERTEC_EMC
R215 1K
SDRAM_CKE
SDRAM_CKE 21:C2
R449 0R
max 200mA

SDRAM 32Mx16
D18
D19

CKE CLK A[0-12] BA0 BA1 CS RAS CAS WE LDQM UDQM
D[0-15]

EMC_AB[2] EMC_AB[3] EMC_AB[4] EMC_AB[5] EMC_AB[6] EMC_AB[7] EMC_AB[8] EMC_AB[9] EMC_AB[10] EMC_AB[11] EMC_AB[12] EMC_AB[13] EMC_AB[14] EMC_AB[0] EMC_AB[1]

D18: EMC_DB[0] EMC_DB[1] EMC_DB[2] EMC_DB[3] EMC_DB[4] EMC_DB[5] EMC_DB[6] EMC_DB[7] EMC_DB[8] EMC_DB[9] EMC_DB[10] EMC_DB[11] EMC_DB[12] EMC_DB[13] EMC_DB[14] EMC_DB[15]
D19: EMC_DB[16] EMC_DB[17] EMC_DB[18] EMC_DB[19] EMC_DB[20] EMC_DB[21] EMC_DB[22] EMC_DB[23] EMC_DB[24] EMC_DB[25] EMC_DB[26] EMC_DB[27] EMC_DB[28] EMC_DB[29] EMC_DB[30] EMC_DB[31]

ERTEC_EMC
R213 10K
C326 15p 50 V
R214 49R9
GND

ERTEC_EMC
R216 10K
C327 15p 50 V
R217 49R9
GND

ERTEC_EMC
J9 E7 D3 C7 B3 A9 A7 VDD
VDD VDD VDDQ VDDQ VDDQ VDD VDDQ
VSS VSSQ VSSQ VSSQ VSSQ VSS VSS
A1 A3 B7 C3 D7 E3 J1
D18
D19
GND

ERTEC_EMC
C328 2u2 16 V
C329 2u2 16 V
C330 2u2 16 V
C331 2u2 16 V
C335 100n 16 V
C336 100n 16 V
C338 100n 16 V
C339 100n 16 V
C341 10n 50 V
C342 10n 50 V
C344 10n 50 V
C345 10n 50 V
C349 1n 50 V
C350 1n 50 V
C352 1n 50 V
C353 1n 50 V
GND

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Memory
SDRAM
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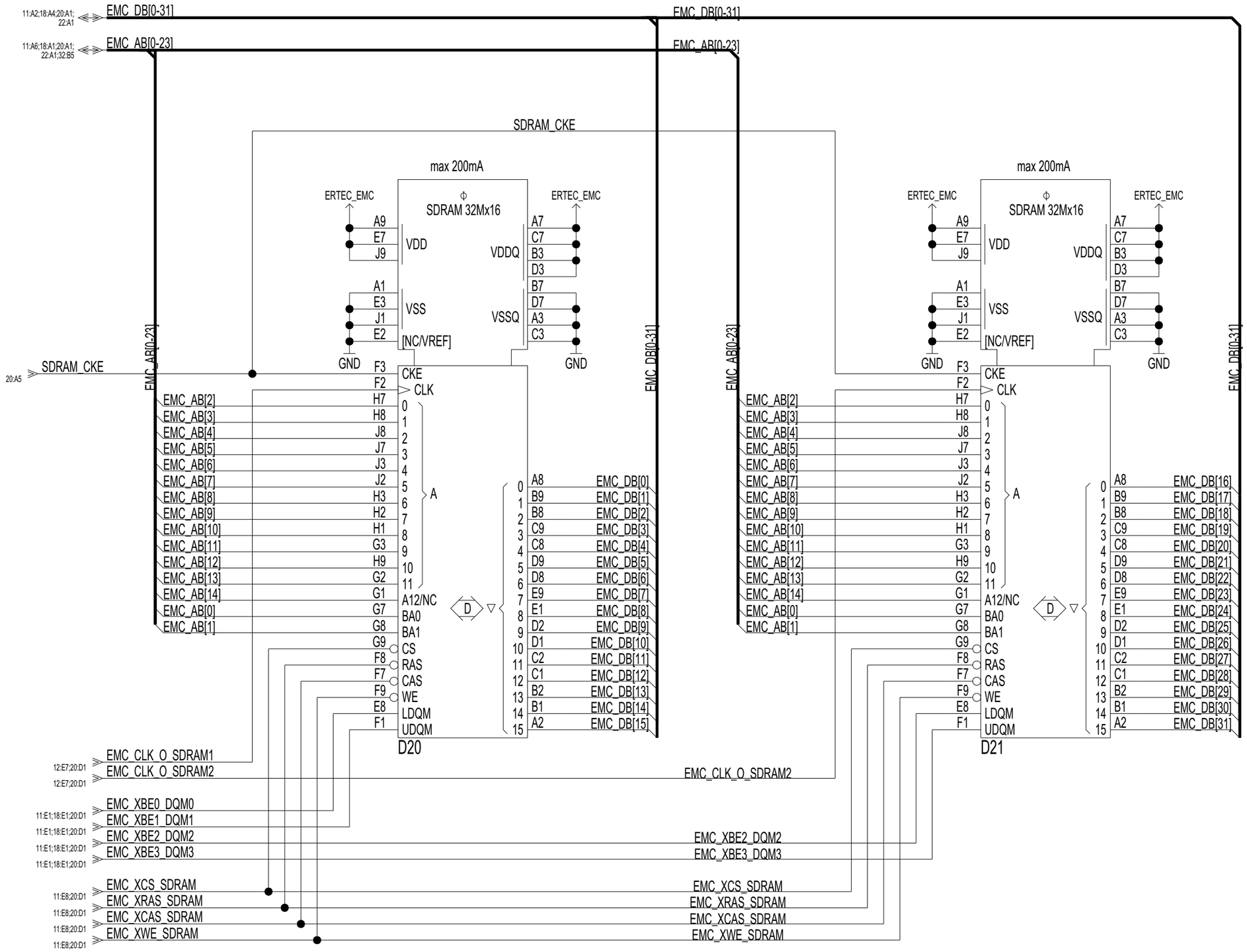
40 Sheets

SDRAM (alternative package)



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EB200P
Memory
SDRAM
Circuit Diagram

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A5E31374985A

Sheet 21
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Burst Mode FLASH

11:A2;18:A4;20:A1; 21:A2 — EMC_DB[0-31]

11:A6;18:A1;20:A1; 21:A2;32:B5 — EMC_AB[0-23]

ERTEC_EMC

R220 1K

R221 1K

max 100mA

FLASH

D22 S29WS128P

D23 S29WS128P

B4	CLK		
G2	0		
F2	1		
E2	2		
D2	3		
F3	4		
E3	5		
D3	6		
C3	7		
C7	8		
E7	9		
F7	10		
C8	11		
D8	12		
E8	13		
F8	14		
D9	15		
G9	16		
F4	17		
E4	18		
D7	19		
E6	20		
E9	21		
F9	22		
F6	23/NC		
G8	24/NC		
H3	OE		
C2	WP		
C5	ACC		
D5	RESET		
C6	WE		
H2	CE		
B2	AVD		
E5	RDY		
		J3	EMC_DB[0]
		G4	EMC_DB[1]
		K4	EMC_DB[2]
		H5	EMC_DB[3]
		H6	EMC_DB[4]
		K7	EMC_DB[5]
		G7	EMC_DB[6]
		J8	EMC_DB[7]
		K3	EMC_DB[8]
		H4	EMC_DB[9]
		J4	EMC_DB[10]
		K5	EMC_DB[11]
		J7	EMC_DB[12]
		H7	EMC_DB[13]
		K8	EMC_DB[14]
		H8	EMC_DB[15]
		J3	EMC_DB[16]
		G4	EMC_DB[17]
		K4	EMC_DB[18]
		H5	EMC_DB[19]
		H6	EMC_DB[20]
		K7	EMC_DB[21]
		G7	EMC_DB[22]
		J8	EMC_DB[23]
		K3	EMC_DB[24]
		H4	EMC_DB[25]
		J4	EMC_DB[26]
		K5	EMC_DB[27]
		J7	EMC_DB[28]
		H7	EMC_DB[29]
		K8	EMC_DB[30]
		H8	EMC_DB[31]

EMC_AB[0-23] EMC_DB[0-31]

R369 10K R358 1K R359 1K

R370 1K

R222 10K R224 10K

C354 15p 50 V C356 15p 50 V

R223 49R9 R225 49R9

R357 0R

R442 0R

R443 0R

EMC_XRESET

EMC_CLK_O_BF1

EMC_CLK_O_BF2

EMC_XCS_PER0

EMC_XWR

EMC_XRD

EMC_XAV_BF

EMC_XRDY_BF

GND

C357 2u2 16 V · C360 100n 16 V · C364 10n 50 V · C368 1n 50 V

C361 100n 16 V · C365 10n 50 V · C369 1n 50 V

C358 2u2 16 V · C362 100n 16 V · C366 10n 50 V · C370 1n 50 V

C696 2u2 16 V · C698 100n 16 V · C701 10n 50 V · C704 1n 50 V

C699 100n 16 V · C702 10n 50 V · C705 1n 50 V

C697 2u2 16 V · C700 100n 16 V · C703 10n 50 V · C706 1n 50 V

L8	VCCQ	VSS	B3
L5	VCC	VSS	G3
J5	VCC	VSS	J9
B6	VCC	VSS	L4
	VCC	VSS	

D22

D23

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EB200P
Memory
Burst mode FLASH
Circuit Diagram

Item No.:

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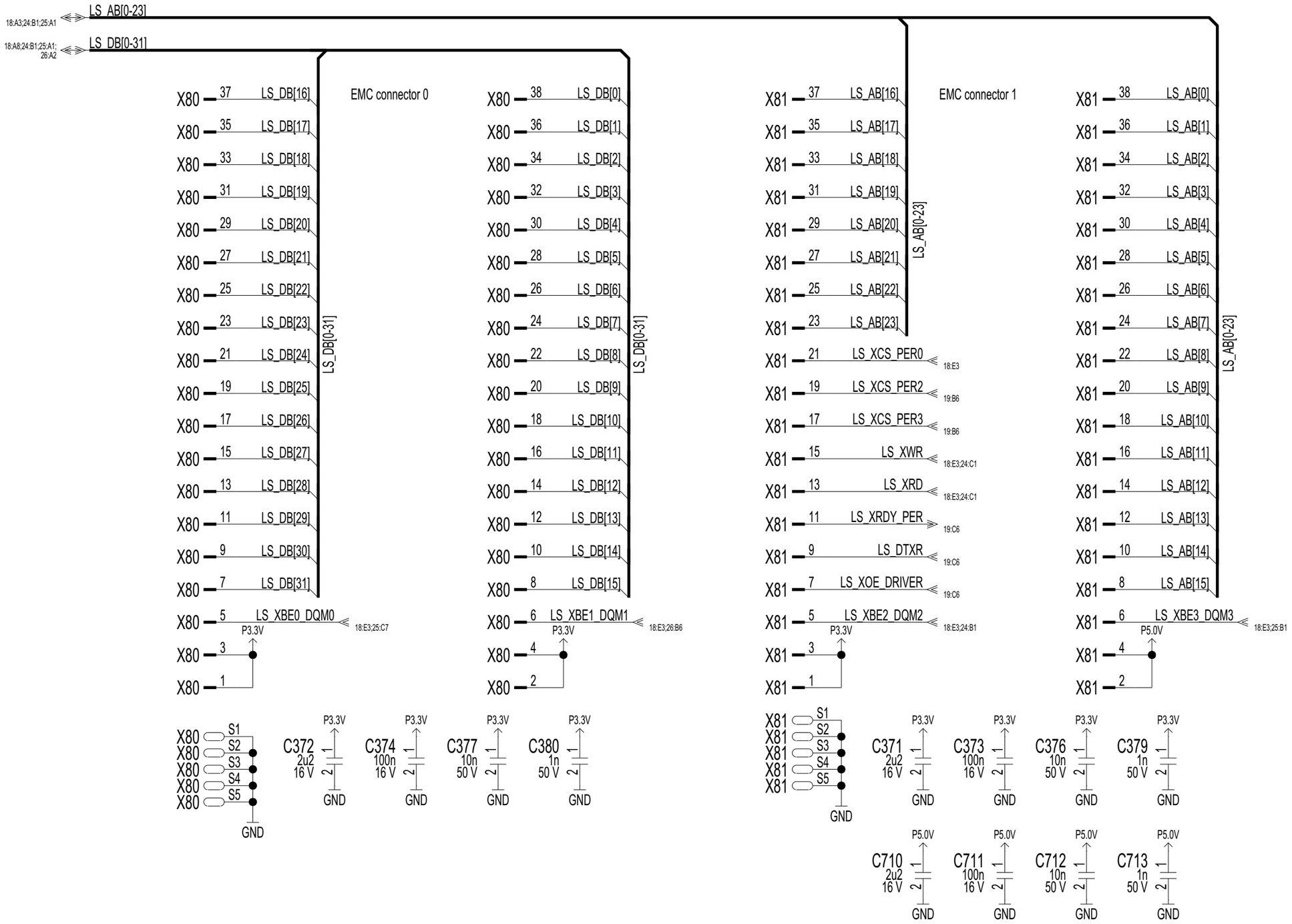
Sheet 22
40 Sheets

EMC connectors



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EB200P
Memory
EMC connectors
Circuit Diagram

Item No.:

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Sheet 23
40 Sheets

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FPGA

Φ ,FPGA

FPGA_TDI
FPGA_TCK
FPGA_TDO
FPGA_TMS
FPGA_CONFIG[3]
LS_XBE2_DQM2
LS_DB[0-31]
LS_AB[0-23]
LS_XWR
LS_XRD

TDI
TCK
TDO
TMS
VCCJ
XRES
VCCIO_0
VCCIO_1
VCCIO-2
VCCIO_2
VREF1-2
VREF2-2
RDQ22
RDQ22
SPLLC_FB_A
SPLLT_FB_A
SPLLC_IN_A
SPLLT_IN_A
PR13A
PR13B
PR14A
PR14B
PCLKT2_0
PCLKC2_0
NC
GNDIO

BANK 2

VCCRX0
HDINP0
VCCIB0
HDINN0
VCCTX0
HDOUTP0
VCCOB0
HDOUTN0
VCCTX1
HDOUTN1
VCCOB1
HDOUTP1
VCCRX1
HDINN1
VCCIB1
HDINP1
AUX33
CLKN
CLKP
VCCP
HDINP2
VCCIB2
HDINN2
VCCRX2
HDOUTP2
VCCOB2
HDOUTN2
VCCTX2
HDOUTN3
VCCOB3
HDOUTP3
VCCTX3
HDINN3
VCCIB3
HDINP3
VCCRX3
VCCAUX
GNDIO

BANK 12

X1_PETp0
X1_PETn0
X1_PERp0
X1_PERn0
REFCLK-
REFCLK+

SERDES input
SERDES output

D1
ECP2M

R236 4K7
R237 10K

P3.3V
FPGA_AUX_P3.3V_A
FPGA_P1.2V_A_O
FPGA_P1.2V_A_I
FPGA_P1.2V_A_S
P1.2V_A
GND

C421 2u2 16 V
C422 100n 16 V
C423 10n 50 V
C424 1n 50 V

Z27 BLM15
Z28 BLM15
Z29 BLM15
Z30 BLM15

C431 100n 16 V
C443 100n 16 V
C432 100n 16 V
C444 100n 16 V
C433 100n 16 V
C445 100n 16 V
C438 100n 16 V
C446 100n 16 V

C451 2u2 16 V
C459 100n 16 V
C467 10n 50 V
C475 1n 50 V
C452 2u2 16 V
C460 100n 16 V
C468 10n 50 V
C476 1n 50 V
C453 2u2 16 V
C461 100n 16 V
C469 10n 50 V
C477 1n 50 V
C454 2u2 16 V
C462 100n 16 V
C470 10n 50 V
C478 1n 50 V
C455 2u2 16 V
C463 100n 16 V
C471 10n 50 V
C479 1n 50 V
C458 2u2 16 V
C466 100n 16 V
C474 10n 50 V
C482 1n 50 V

C403 2u2 16 V
C407 100n 16 V
C413 10n 50 V
C417 1n 50 V
C404 2u2 16 V
C408 100n 16 V
C414 10n 50 V
C418 1n 50 V
C405 2u2 16 V
C409 100n 16 V
C415 10n 50 V
C419 1n 50 V
C406 2u2 16 V
C410 100n 16 V
C416 10n 50 V
C420 1n 50 V

C426 2u2 16 V
C434 100n 16 V
C439 10n 50 V
C447 1n 50 V
C427 2u2 16 V
C435 100n 16 V
C440 10n 50 V
C448 1n 50 V
C428 2u2 16 V
C436 100n 16 V
C441 10n 50 V
C449 1n 50 V
C429 2u2 16 V
C437 100n 16 V
C442 10n 50 V
C450 1n 50 V

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EB200P
FPGA
FPGA
Circuit Diagram

Item No.:

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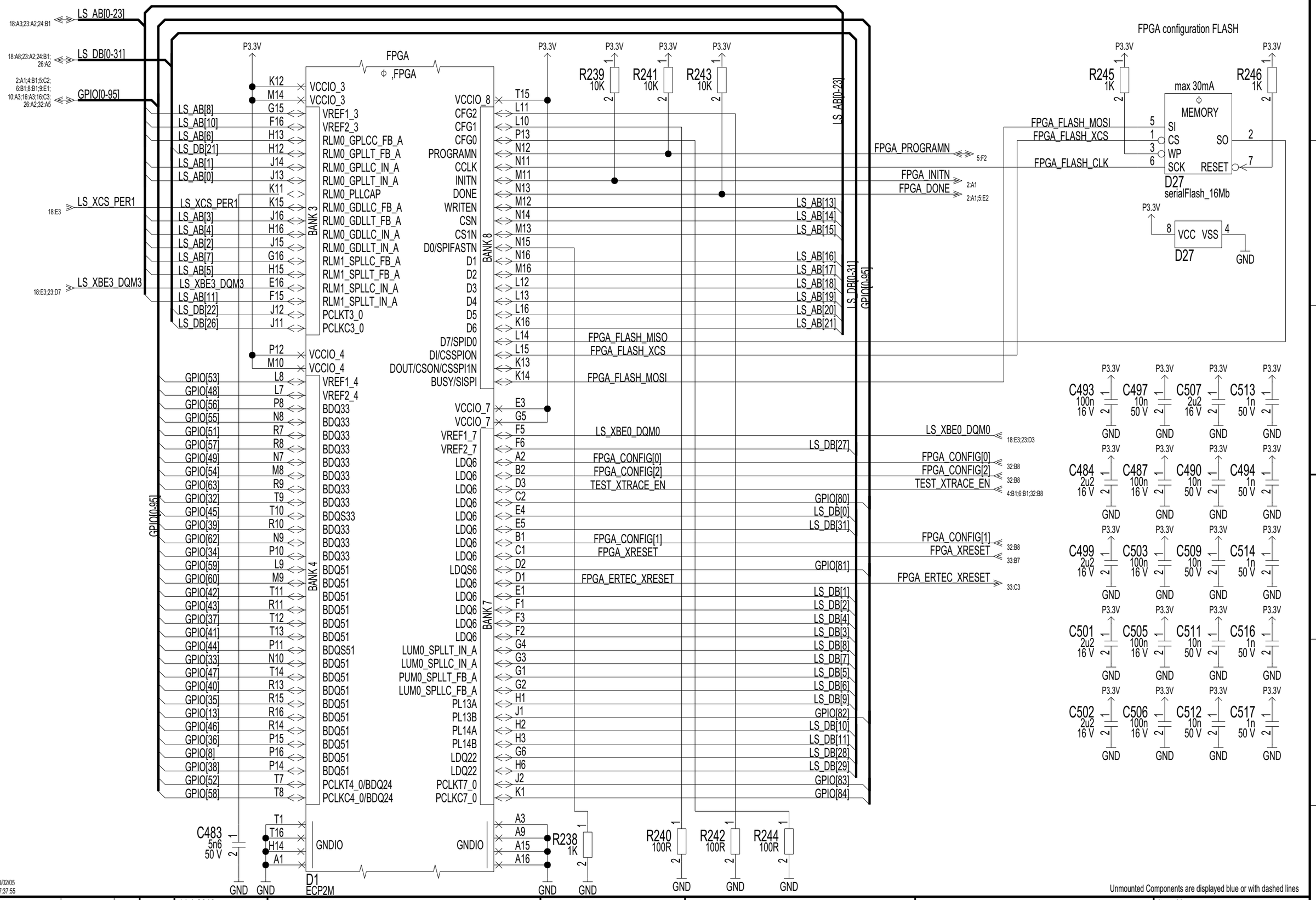
Sheet 24
40 Sheets



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					Appr.	
					Norm	

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EB200P
FPGA
FPGA
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40 Sheets

2:A1;4:B1;5:C2;
6:B1;8:B1;9:E1;
10:A3;16:A3;16:C3;
25:A1;32:A5

GPIO[0-95]

18:A8;23:A2;24:B1;
25:A1

LS_DB[0-31]

GPIO[0-95]

GPIO[0-95]

LS_DB[0-31]

GPIO[0-95]

P1.2V

FPGA_P1.2V_A

FPGA

P3.3V

P3.3V

Φ ,FPGA

M7 VCCIO_5
P5 VCCIO_5
R6 VREF1_5
T6 VREF2_5
M5 BDQ6
N5 BDQ6
L6 BDQ6
M6 BDQ6
P3 BDQ6
P4 BDQ6
P2 BDQ6
P1 BDQ6
R1 BDQS6
R2 BDQ6
R3 BDQ6
T2 BDQ6
R4 BDQ6
T3 BDQ6
T4 BDQ6
T5 BDQ6
P6 PCLKT5_0
P7 PCLKC5_0

BANK 5

GPIO[79]
GPIO[61]
GPIO[73]
GPIO[74]
GPIO[76]
GPIO[77]
GPIO[67]
GPIO[70]
GPIO[64]
GPIO[94]
GPIO[95]
GPIO[65]
GPIO[68]
GPIO[66]
GPIO[71]
GPIO[69]
GPIO[72]
GPIO[75]
GPIO[78]
GPIO[50]

B6 GNDIO
B12 GNDIO
E2 GNDIO
E15 GNDIO

GND

D1
ECP2M

K5 VCCIO_6
M3 VCCIO_6
K4 VREF1_6
J4 VREF2_6
M1 GDLLT_IN_A
N2 GDLLT_FB_A
N1 GDLLC_IN_A
N3 GDLLC_FB_A
L1 GPLLT_IN_A
L3 GPLLT_FB_A
L2 GPLLC_IN_A
L4 GPLLC_FB_A
J6 SPLLT_IN_A
K3 SPLLT_FB_A
J5 SPLLC_IN_A
K2 SPLLC_FB_A
M4 PLLCAP
H5 PCLKC6_0
H4 PCLKT6_0

BANK 6

LS_XBE1_DQM1
18:E3;23:D4

LS_DB[14]
GPIO[90]
GPIO[92]
GPIO[91]
GPIO[93]

FPGA_INFO
2:A1

GPIO[88]
GPIO[87]
GPIO[89]

LS_DB[30]
GPIO[86]

LS_DB[15]
GPIO[85]

LS_DB[13]
LS_DB[12]

G10 VCCPLL
G7 VCC
G9 VCC
H7 VCC
J10 VCC
K10 VCC
K8 VCC

C522
5n6
50 V

GND

P1.2V_A

FPGA_P1.2V_A

C528
100n
16 V

Z33
BLM15

C532
100n
16 V

GND

GND

P3.3V

C544 100n 16 V — GND
C553 10n 50 V — GND
C562 1n 50 V — GND
C545 100n 16 V — GND
C554 10n 50 V — GND
C563 1n 50 V — GND

P1.2V

C537 2u2 16 V — GND
C546 100n 16 V — GND
C555 10n 50 V — GND
C564 1n 50 V — GND
C538 2u2 16 V — GND
C547 100n 16 V — GND
C556 10n 50 V — GND
C565 1n 50 V — GND
C539 2u2 16 V — GND
C548 100n 16 V — GND
C557 10n 50 V — GND
C566 1n 50 V — GND

FPGA_P1.2V_A

C543 2u2 16 V — GND
C552 100n 16 V — GND
C561 10n 50 V — GND
C570 1n 50 V — GND

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EB200P
FPGA
FPGA
Circuit Diagram

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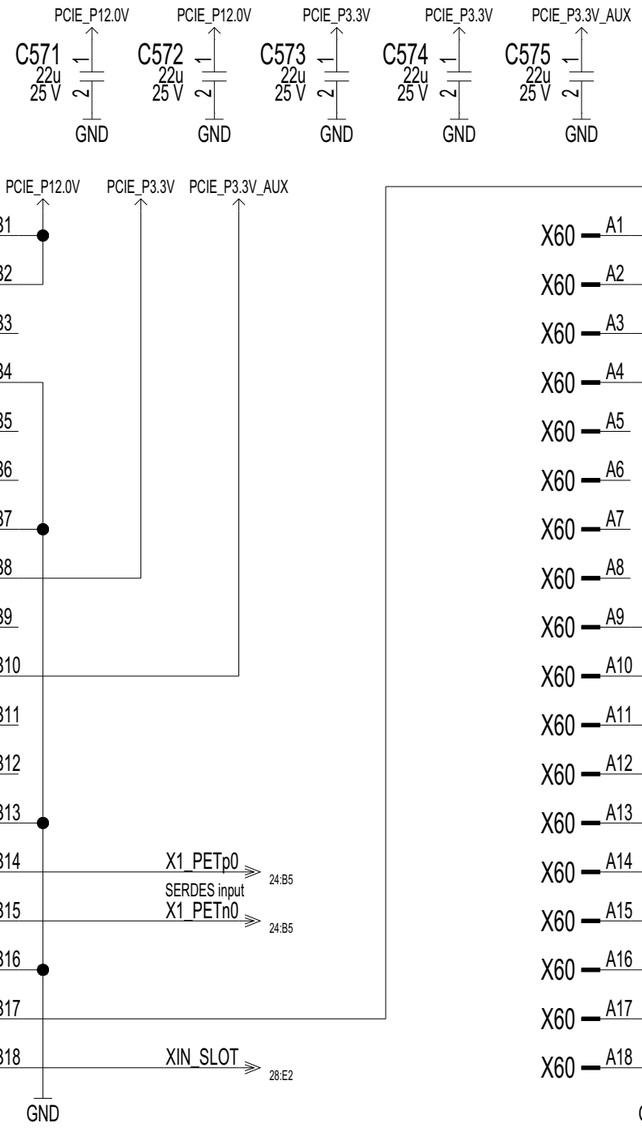
PCIe Connector X1



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EB200P
Interfaces
PCIe board connector
Circuit Diagram

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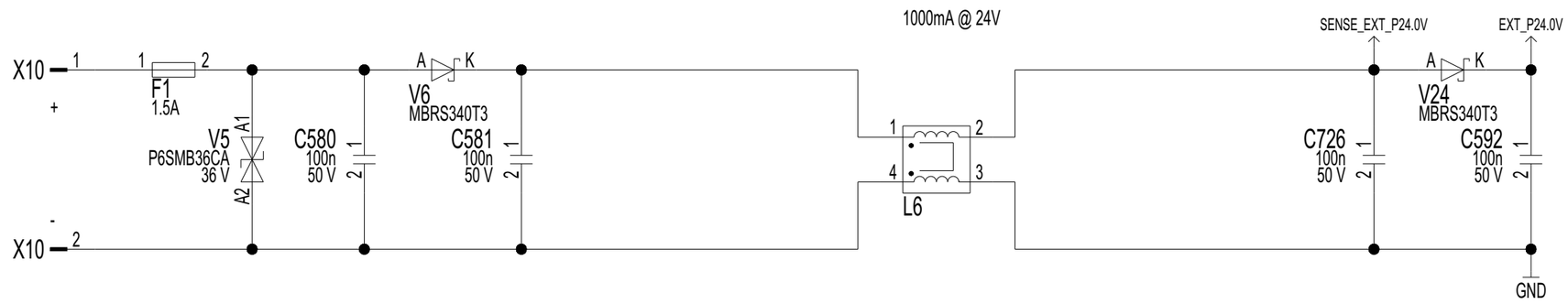
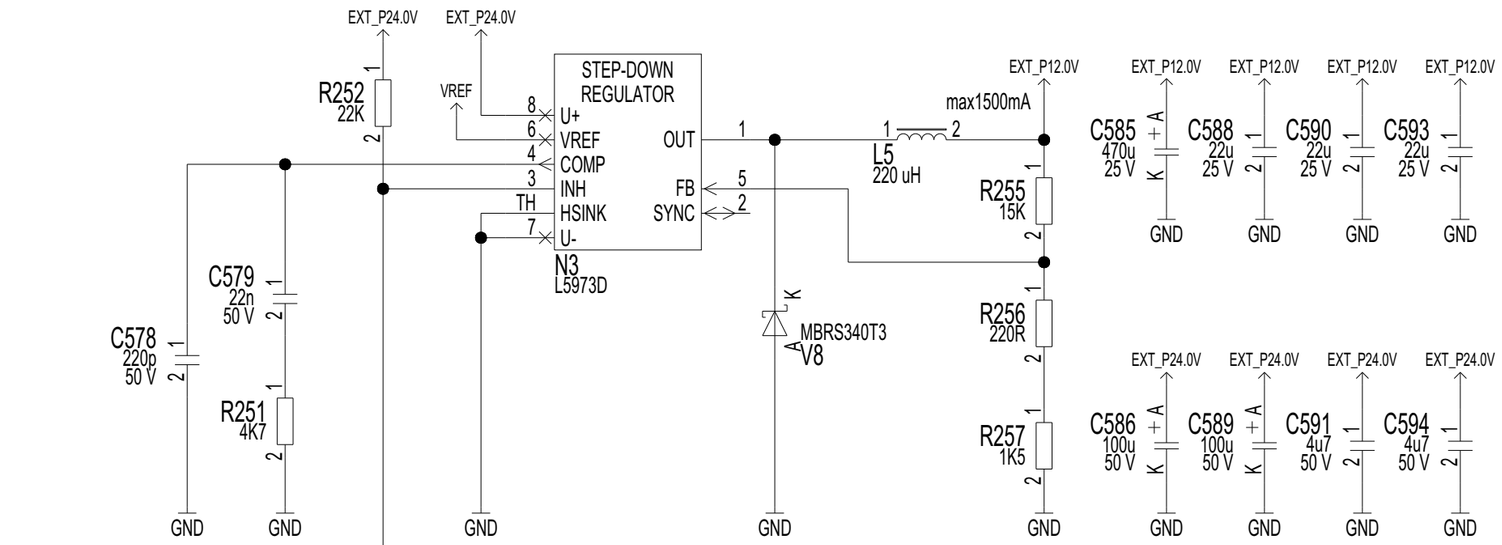
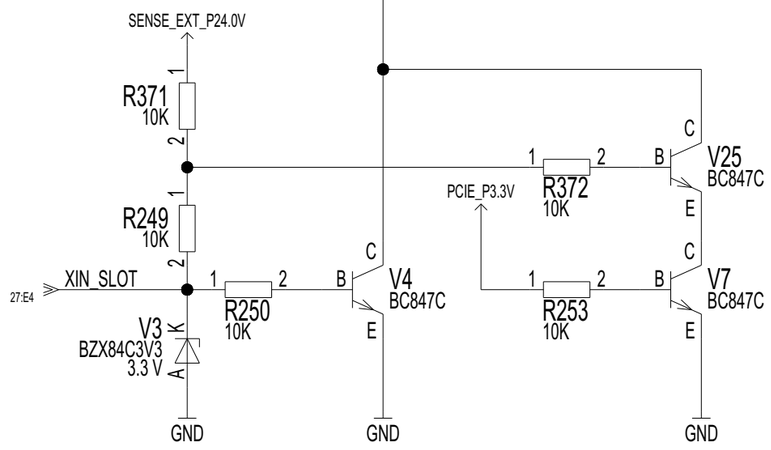
Sheet 27
40 Sheets

External power supply input and convertor



24V to 12V convertor





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					Appr.	
					Norm	

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EB200P
Power supply
External power input
Circuit Diagram

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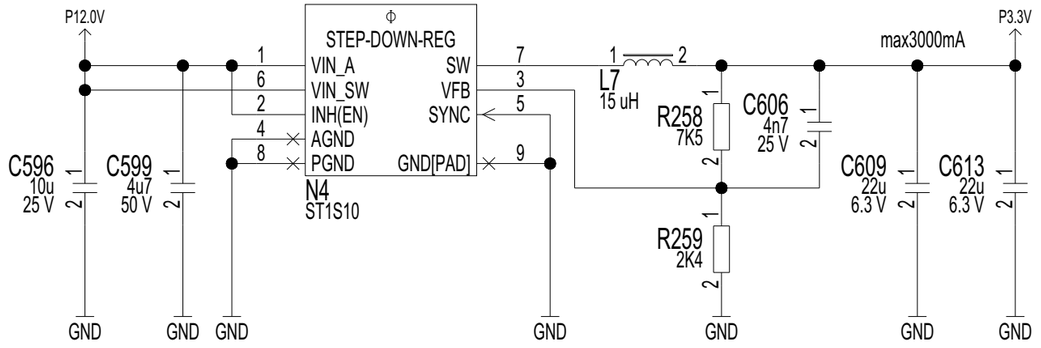
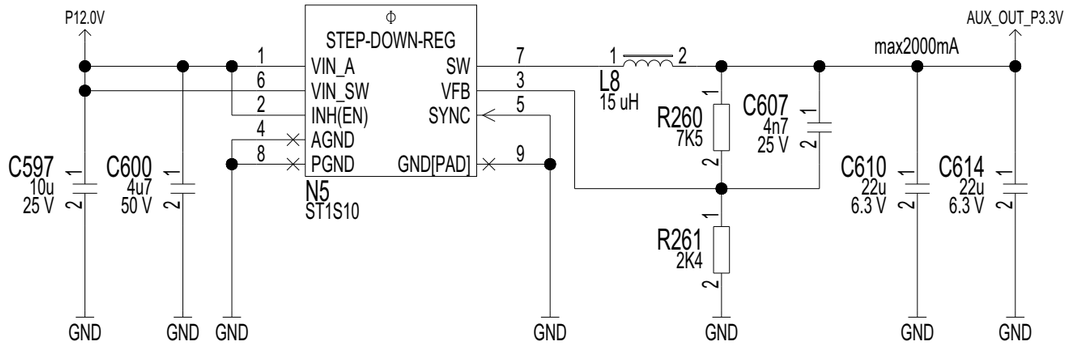
Power supply convertors

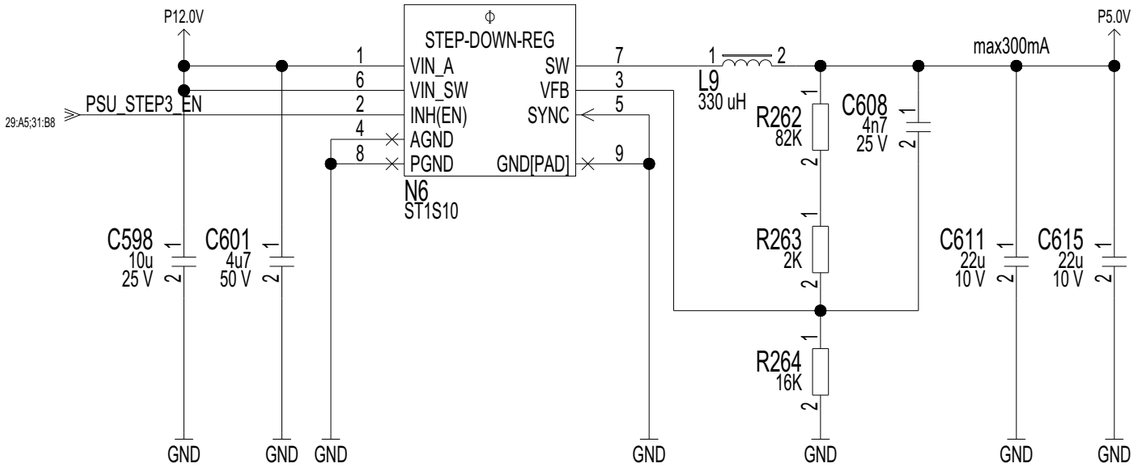
12V to 3.3V convertor



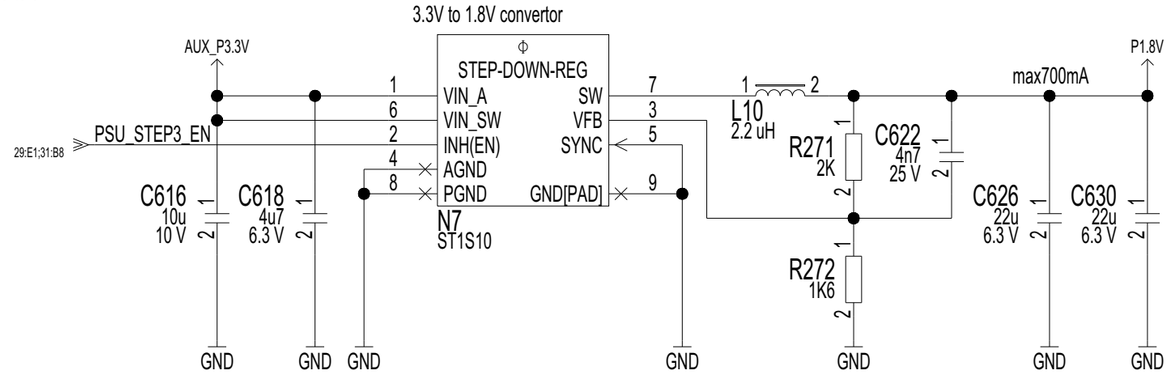
12V to 3.3V convertor (aux)



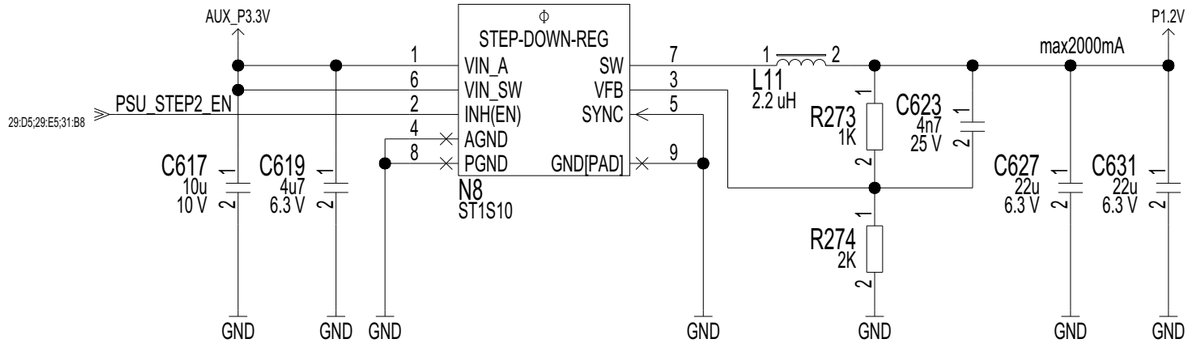
12V to 5.0V convertor



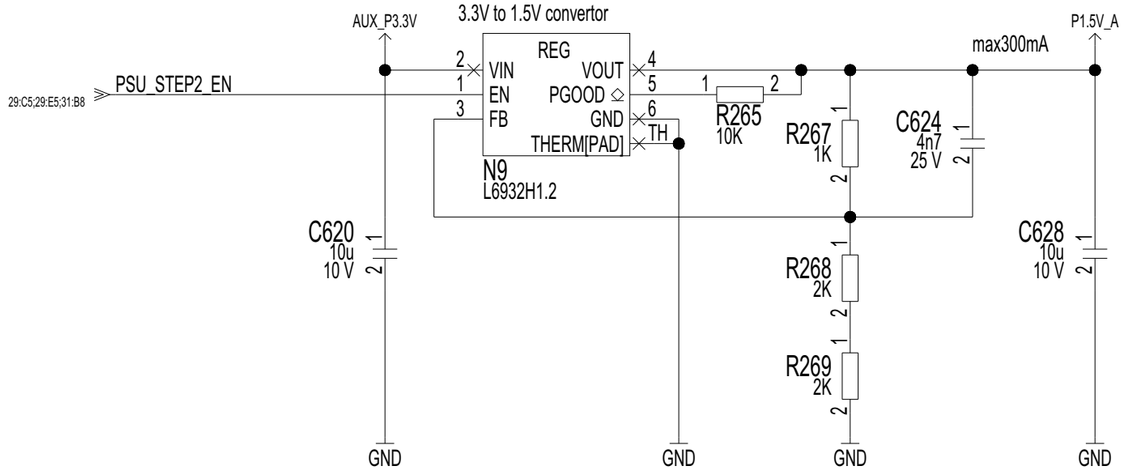
3.3V to 1.8V convertor



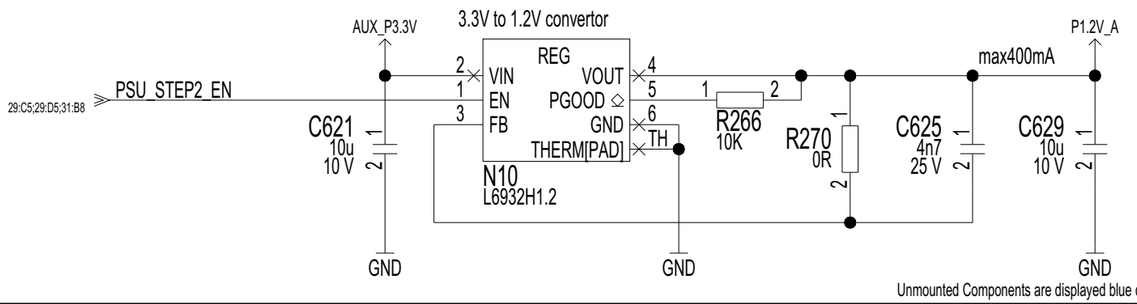
3.3V to 1.2V convertor



3.3V to 1.5V convertor



3.3V to 1.2V convertor



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Date	14.1.2013
Init.	
Appr.	
Norm	

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EB200P
Power supply
Power convertors
Circuit Diagram

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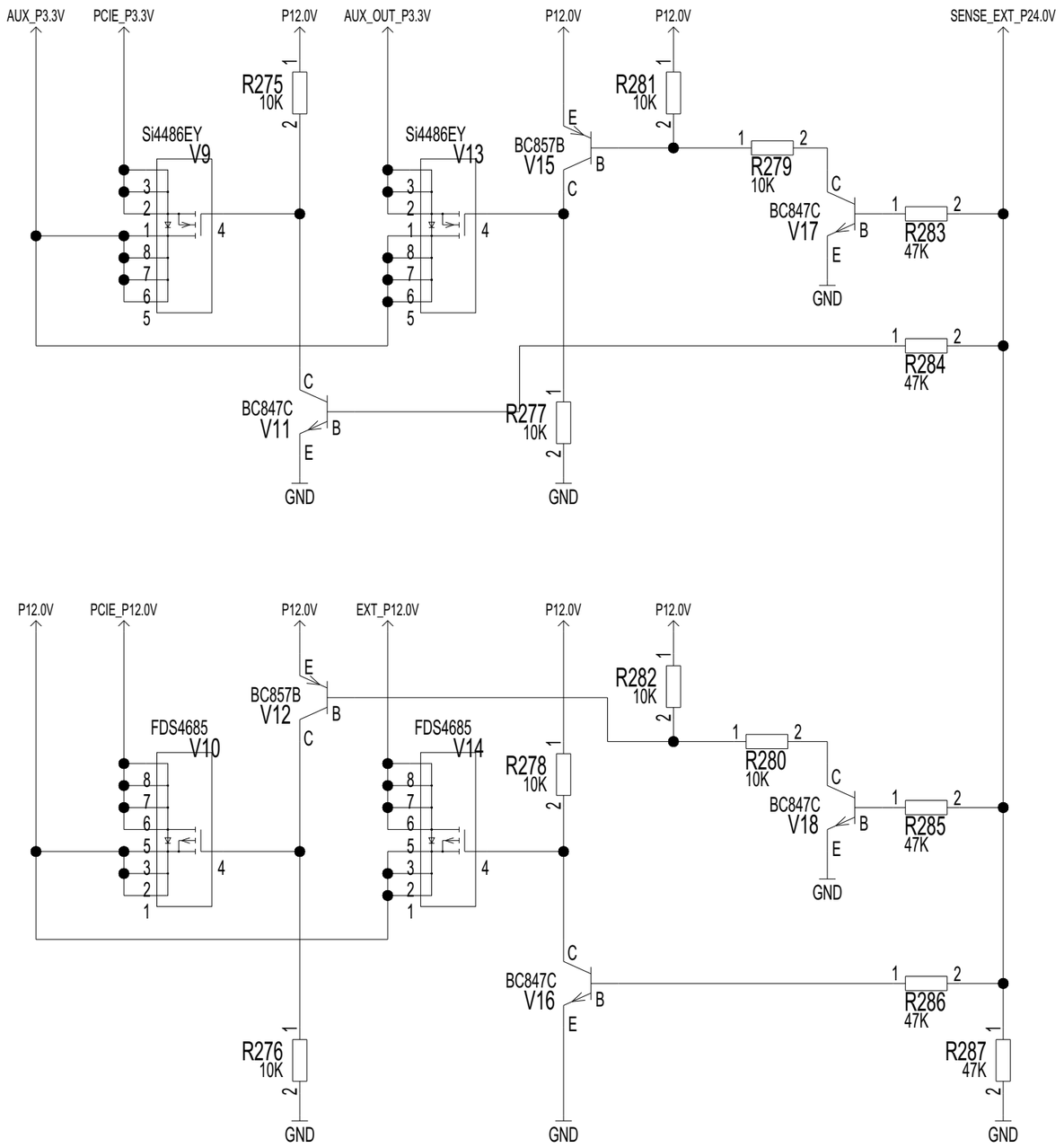
Power switches



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					Appr.	
					Norm	

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EB200P
Power supply
Power switching
Circuit Diagram

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Sheet 30
40 Sheets

Power sensing circuits

P1.2V
R373 22R
R288 470R
R289 1K2
R290 56R
GND
P0.8V
P2.5V
COMP
U1 2901
R301 3K3
BAS40-07 V20
R298 100K
PWR_STEP3_EN
PWR_PG

P1.2V_A
R374 22R
R291 470R
R292 1K2
R293 56R
GND
P0.8V
P2.5V
COMP
U1 2901
R302 3K3
BAS40-07 V21
R299 100K
PWR_STEP3_EN
PWR_PG

P1.8V
R295 680R
R296 56R
R297 680R
GND
P0.8V
P2.5V
COMP
U2 2901
R303 3K3
V19 BAS40-07
R300 100K
PWR_PG

P1.5V_A
R307 560R
R308 56R
R309 10R
R376 820R
GND
P0.8V
P2.5V
COMP
U2 2901
R319 3K3
R315 100K
BAS40-07 V22
PWR_STEP3_EN
PWR_PG

P3.3V
R377 120R
R304 3K9
R310 1K8
R311 470R
R379 10R
GND
P0.8V
P2.5V
COMP
U2 2901
R320 3K3
R317 100K
BAS40-07 V23
PWR_STEP2_EN
PWR_PG

P5.0V
R375 1K5
R305 560R
R312 18K
R313 39R
R378 390R
GND
P0.8V
P2.5V
COMP
U2 2901
R321 3K3
R316 100K
V19 BAS40-07
PWR_PG

Voltage reference

P12.0V
R326 1K2
max5mA
N11 431
R328 10K
R330 2K7
R329 1K
GND
P2.5V
P0.8V

P12.0V
COMP
U1 2901
max5mA
VCC GND
U1
GND

P12.0V
COMP
U2 2901
max5mA
VCC GND
U2
GND

AUX_P3.3V
max5mA
VCC GND
D28
D29
D30
GND

C640 100n 16 V
C643 10n 50 V
C646 100n 16 V
C650 10n 16 V
C647 100n 16 V
C651 10n 50 V

R323 10K
R322 10K
R324 10K
R325 1K
R327 1K
R380 22K
R381 22K
R382 22K

D28 74LVC1G07
D29 74LVC1G07
D30 74LVC1G07

PSU_STEP3_EN → 29:E1;29:A5
PSU_STEP2_EN → 29:C5;29:D5;29:E5
PSU_PG → 2:A1;33:B3

C632 10u 10 V
C634 100n 16 V
C636 10n 50 V
C638 1n 50 V
C641 10u 10 V
C644 100n 16 V
C648 10n 50 V
C652 1n 50 V

C633 10u 25 V
C635 100n 16 V
C637 10n 50 V
C639 1n 50 V
C642 10u 25 V
C645 100n 16 V
C649 10n 50 V
C653 1n 50 V

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Ind.	Rev.	Modification	Date	Name		
	002				Date	14.1.2013
					Init.	
					Appr.	
					Norm	

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EB200P
Power supply
Power sensing
Circuit Diagram

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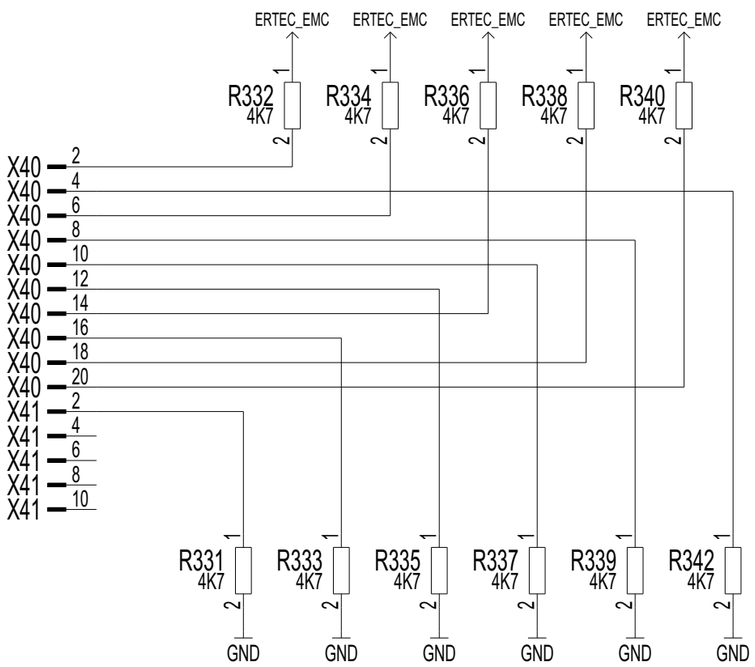
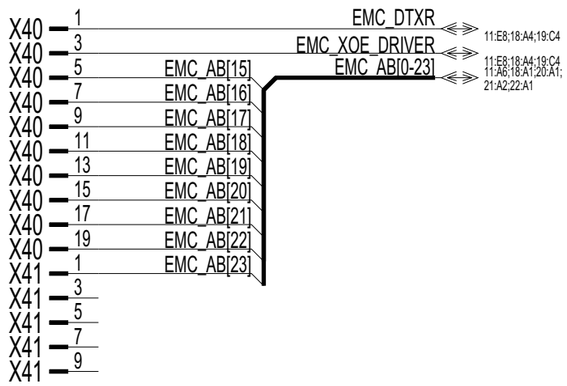
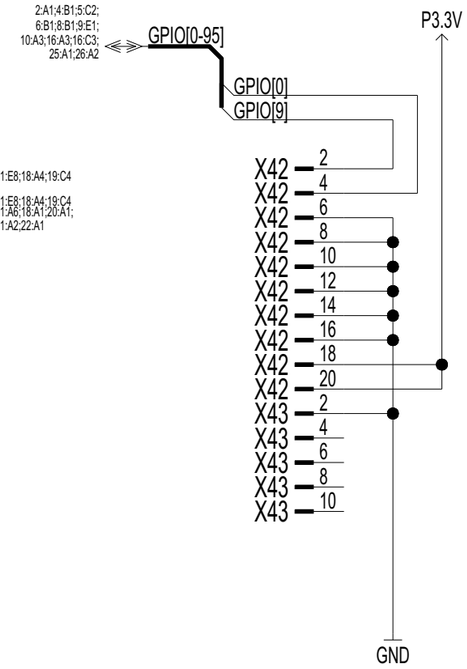
Configuration jumpers

ERTEC 200P jumpers

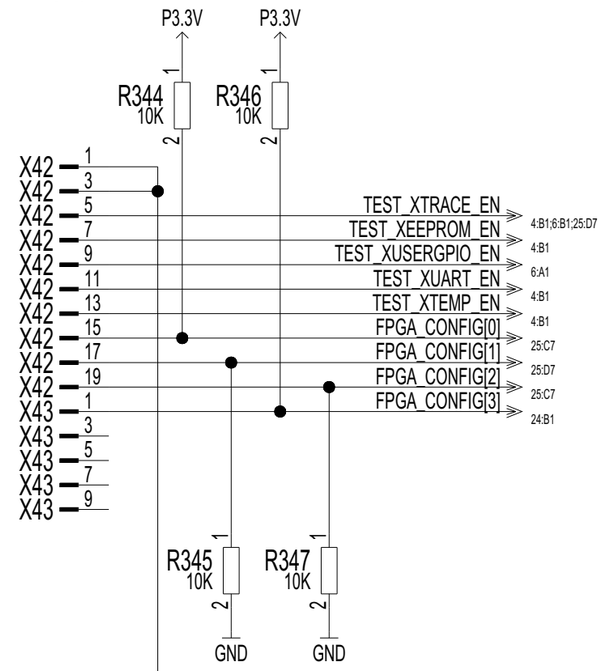


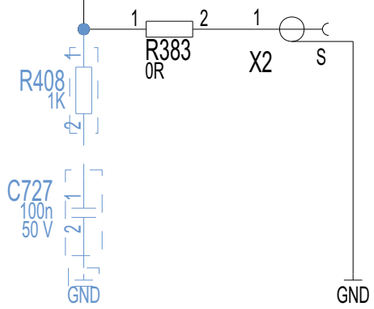




Pin	Function	Signal
01	Boot(0)	ERTEC EMC DTXR
03	Boot(1)	ERTEC EMC XOE_DRIVER
05	Boot(2)	ERTEC EMC A15
07	Boot(3)	ERTEC EMC A16
09	Config(0)	ERTEC EMC A17
11	Config(1)	ERTEC EMC A18
13	Config(2)	ERTEC EMC A19
15	Config(3)	ERTEC EMC A20
17	Config(4)	ERTEC EMC A21
19	Config(5)	ERTEC EMC A22
21(01)	Config(6)	ERTEC EMC A23
23(03)	None	NC
25(05)	None	NC
27(07)	None	NC
29(09)	None	NC

FPGA jumpers





Pin	Function	Signal
01	Sync(0)	BNC tip pin
03	Sync(1)	BNC tip pin
05	Trace	Trace CS bus switch OE
07	EEPROM	EEPROM CS bus switch OE
09	User	GPIOs User GPIOs CS bus switch OE
11	UART	UART CS bus switch OE
13	TEMP	TEMP CS bus switch OE
15	F_XHIF(0)	FPGA_CONFIG(0)
17	F_XHIF(1)	FPGA_CONFIG(1)
19	F_XHIF(2)	FPGA_CONFIG(2)
21(01)	F_XHIF(3)	FPGA_CONFIG(3)
23(03)	None	NC
25(05)	None	NC
27(07)	None	NC
29(09)	None	NC

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EB200P
Configuration
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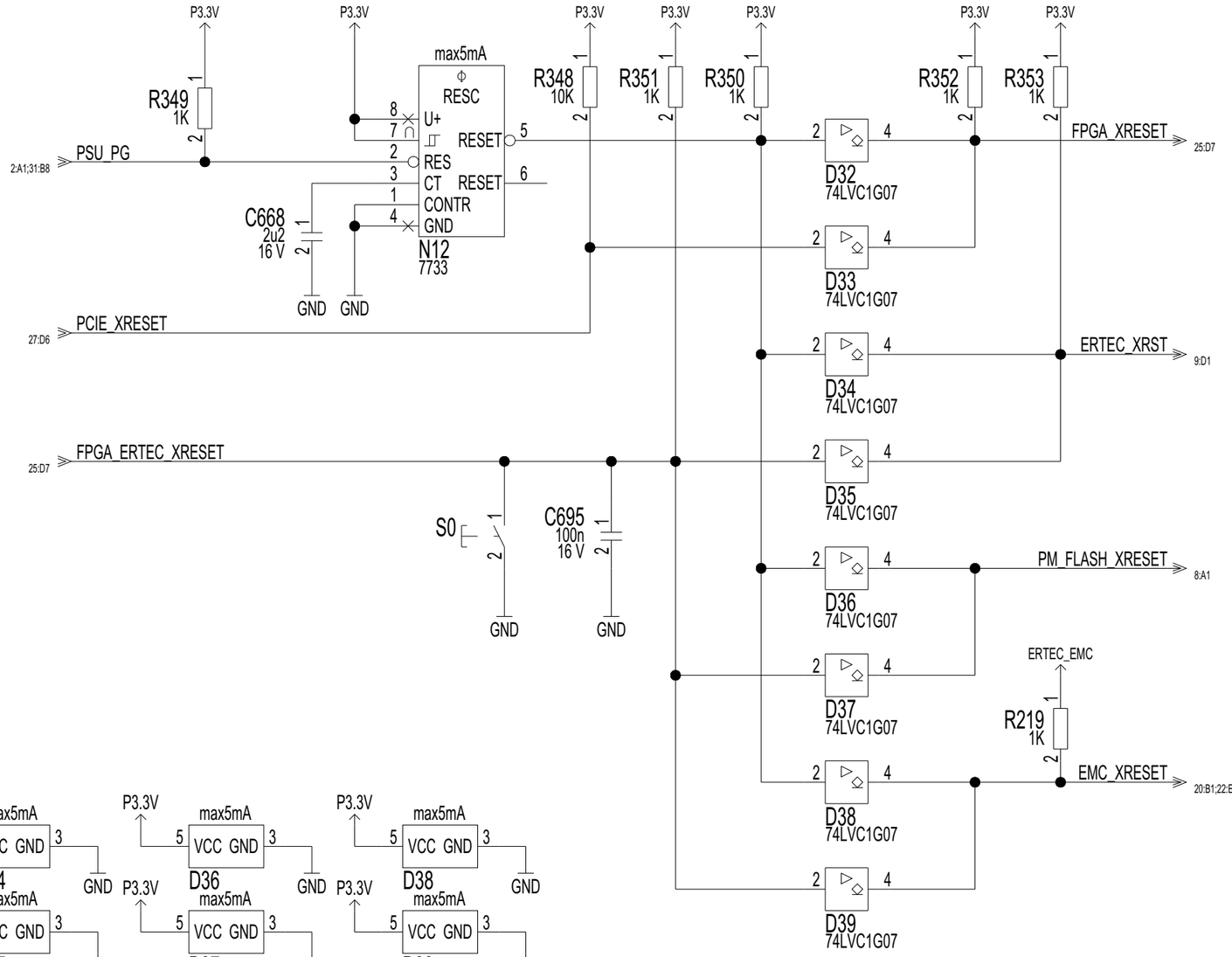
Reset circuit



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EB200P
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X1 PIN.NO	A NETNAME	B NETNAME	C NETNAME	D NETNAME
1	P1_TXP	P2_TXP	TAPA_P	TAPB_P
2	P1_TXN	P2_TXN	TAPA_N	TAPB_N
3	P1_RXP	P2_RXP	SIGN592	SIGN593
4	SIGN587	SIGN585	SIGN594	SIGN596
5	SIGN586	SIGN584	SIGN595	SIGN597
6	P1_RXN	P2_RXN	SIGN591	SIGN590
7				
8	EARTH	EARTH	EARTH	EARTH
9	SIGN580	SIGN582		
10	P1_LINK	P2_LINK		
11	SIGN581	SIGN583		
12	P1_ACT	P2_ACT		

X1 PIN.NO	SHIELDPINS NETNAME
S1	EARTH
S	EARTH
S2	EARTH
S3	EARTH
S4	EARTH

X10 PIN.NO	NETNAME
1	SIGN354
2	INPUT_GROUND

X11 PIN.NO	NETNAME
1	SIGN111
2	SIGN113
3	SIGN112
4	
5	SIGN110

X11 PIN.NO	SHIELDPINS NETNAME
S	SIGN490

X12 PIN.NO	NETNAME
1	SYNC_P
2	SYNC_N
3	SIGN95

X2 PIN.NO	NETNAME
1	SIGN640
COP1	
COP2	

X2 PIN.NO	SHIELDPINS NETNAME
S	GND

X20 PIN.NO	NETNAME
1	P3.3V
2	P5.0V
3	P3.3V
4	P5.0V
5	PM_FLASH_XRESET
6	
7	GPIO[31]
8	GPIO[15]
9	GPIO[30]
10	GPIO[14]
11	GPIO[29]
12	GPIO[13]
13	GPIO[28]
14	GPIO[12]
15	GPIO[27]
16	GPIO[11]
17	GPIO[26]
18	GPIO[10]
19	GPIO[25]
20	GPIO[9]
21	GPIO[24]
22	GPIO[8]
23	GPIO[23]
24	GPIO[7]
25	GPIO[22]
26	GPIO[6]
27	GPIO[21]
28	GPIO[5]
29	GPIO[20]
30	GPIO[4]
31	GPIO[19]
32	GPIO[3]
33	GPIO[18]
34	GPIO[2]
35	GPIO[17]
36	GPIO[1]
37	GPIO[16]
38	GPIO[0]

X20 PIN.NO	SHIELDPINS NETNAME
S1	GND
S2	GND
S3	GND
S4	GND
S5	GND

X21 PIN.NO	NETNAME
1	P3.3V
2	P5.0V
3	P3.3V
4	P5.0V
5	ERTEC_REF_CLK
6	
7	GPIO[63]
8	GPIO[47]
9	GPIO[62]
10	GPIO[46]
11	GPIO[61]
12	GPIO[45]
13	GPIO[60]
14	GPIO[44]
15	GPIO[59]
16	GPIO[43]
17	GPIO[58]
18	GPIO[42]
19	GPIO[57]
20	GPIO[41]
21	GPIO[56]
22	GPIO[40]
23	GPIO[55]
24	GPIO[39]
25	GPIO[54]
26	GPIO[38]
27	GPIO[53]
28	GPIO[37]
29	GPIO[52]
30	GPIO[36]
31	GPIO[51]
32	GPIO[35]
33	GPIO[50]
34	GPIO[34]
35	GPIO[49]
36	GPIO[33]
37	GPIO[48]
38	GPIO[32]

X21 PIN.NO	SHIELDPINS NETNAME
S1	GND
S2	GND
S3	GND
S4	GND
S5	GND

X22 PIN.NO	NETNAME
1	P3.3V
2	P5.0V
3	P3.3V
4	P5.0V
5	
6	
7	GPIO[95]
8	GPIO[79]
9	GPIO[94]
10	GPIO[78]
11	GPIO[93]
12	GPIO[77]
13	GPIO[92]
14	GPIO[76]
15	GPIO[91]
16	GPIO[75]
17	GPIO[90]
18	GPIO[74]
19	GPIO[89]
20	GPIO[73]
21	GPIO[88]
22	GPIO[72]
23	GPIO[87]
24	GPIO[71]
25	GPIO[86]
26	GPIO[70]
27	GPIO[85]
28	GPIO[69]
29	GPIO[84]
30	GPIO[68]
31	GPIO[83]
32	GPIO[67]
33	GPIO[82]
34	GPIO[66]
35	GPIO[81]
36	GPIO[65]
37	GPIO[80]
38	GPIO[64]

X22 PIN.NO	SHIELDPINS NETNAME
S1	GND
S2	GND
S3	GND
S4	GND
S5	GND

X30 PIN.NO	NETNAME
1	
2	
3	
4	
5	
6	TRACECLK
7	TRACE_DBGRQ
8	TRACE_DBACK
9	ERTEC_XSRST
10	
11	ERTEC_TDO
12	P3.3V
13	ERTEC_RTCK
14	P3.3V
15	ERTEC_TCK
16	TRACEPKT[7]
17	ERTEC_TMS
18	TRACEPKT[6]
19	ERTEC_TDI
20	TRACEPKT[5]
21	ERTEC_XTRST
22	TRACEPKT[4]
23	TRACEPKT[15]
24	TRACEPKT[3]
25	TRACEPKT[14]
26	TRACEPKT[2]
27	TRACEPKT[13]
28	TRACEPKT[1]
29	TRACEPKT[12]
30	TRACEPKT[0]
31	TRACEPKT[11]
32	TRACESYNC
33	TRACEPKT[10]
34	PIPESTAT[2]
35	TRACEPKT[9]
36	PIPESTAT[1]
37	TRACEPKT[8]
38	PIPESTAT[0]

X30 PIN.NO	SHIELDPINS NETNAME
S1	GND
S2	GND
S3	GND
S4	GND
S5	GND

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EB200P
CONNECTOR TABLES
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X31 PIN.NO	NETNAME
1	P3.3V
2	P3.3V
3	ERTEC_XTRST
4	GND
5	ERTEC_TDI
6	GND
7	ERTEC_TMS
8	GND
9	ERTEC_TCK
10	GND
11	ERTEC_RTCK
12	GND
13	ERTEC_TDO
14	GND
15	ERTEC_XSRST
16	GND
17	JTAG_DBGRQ
18	GND
19	JTAG_DBACK
20	GND

X40 PIN.NO	NETNAME
1	EMC_DTXR
2	SIGN515
3	EMC_XOE_DRIVER
4	SIGN520
5	EMC_AB[15]
6	SIGN516
7	EMC_AB[16]
8	SIGN521
9	EMC_AB[17]
10	SIGN522
11	EMC_AB[18]
12	SIGN523
13	EMC_AB[19]
14	SIGN517
15	EMC_AB[20]
16	SIGN524
17	EMC_AB[21]
18	SIGN518
19	EMC_AB[22]
20	SIGN519

X43 PIN.NO	NETNAME
1	FPGA_CONFIG[3]
2	GND
3	
4	
5	
6	
7	
8	
9	
10	

X60 PIN.NO	A NETNAME	B NETNAME
1	SIGN351	PCIE_P12.0V
2	PCIE_P12.0V	PCIE_P12.0V
3	PCIE_P12.0V	
4	GND	GND
5		
6		
7		GND
8		PCIE_P3.3V
9	PCIE_P3.3V	
10	PCIE_P3.3V	PCIE_P3.3V_AUX
11	PCIE_XRESET	
12	GND	
13	REFCLK+	GND
14	REFCLK-	X1_PETp0
15	GND	X1_PETn0
16	SIGN352	GND
17	SIGN353	SIGN351
18	GND	XIN_SLOT

X80 PIN.NO	NETNAME
1	P3.3V
2	P3.3V
3	P3.3V
4	P3.3V
5	LS_XBE0_DQM0
6	LS_XBE1_DQM1
7	LS_DB[31]
8	LS_DB[15]
9	LS_DB[30]
10	LS_DB[14]
11	LS_DB[29]
12	LS_DB[13]
13	LS_DB[28]
14	LS_DB[12]
15	LS_DB[27]
16	LS_DB[11]
17	LS_DB[26]
18	LS_DB[10]
19	LS_DB[25]
20	LS_DB[9]
21	LS_DB[24]
22	LS_DB[8]
23	LS_DB[23]
24	LS_DB[7]
25	LS_DB[22]
26	LS_DB[6]
27	LS_DB[21]
28	LS_DB[5]
29	LS_DB[20]
30	LS_DB[4]
31	LS_DB[19]
32	LS_DB[3]
33	LS_DB[18]
34	LS_DB[2]
35	LS_DB[17]
36	LS_DB[1]
37	LS_DB[16]
38	LS_DB[0]

X80 PIN.NO	SHIELDPINS NETNAME
S1	GND
S2	GND
S3	GND
S4	GND
S5	GND

X32 PIN.NO	NETNAME
1	FPGA_TCK
2	GND
3	FPGA_TMS
4	GND
5	FPGA_TDI
6	P3.3V
7	FPGA_TDO
8	GND
9	FPGA_DONE
10	FPGA_PROGRAMN

X42 PIN.NO	NETNAME
1	SIGN529
2	GPIO[9]
3	SIGN529
4	GPIO[0]
5	TEST_XTRACE_EN
6	GND
7	TEST_XEEPROM_EN
8	GND
9	TEST_XUSERGPIO_EN
10	GND
11	TEST_XUART_EN
12	GND
13	TEST_XTEMP_EN
14	GND
15	FPGA_CONFIG[0]
16	GND
17	FPGA_CONFIG[1]
18	P3.3V
19	FPGA_CONFIG[2]
20	P3.3V

X50 PIN.NO	NETNAME
1	GND
2	GND
3	USER_GPIO[0]
4	USER_GPIO[1]
5	USER_GPIO[2]
6	USER_GPIO[3]
7	USER_GPIO[4]
8	USER_GPIO[5]
9	USER_GPIO[6]
10	USER_GPIO[7]
11	USER_GPIO[8]
12	USER_GPIO[9]
13	USER_GPIO[10]
14	USER_GPIO[11]
15	USER_GPIO[12]
16	USER_GPIO[13]
17	USER_GPIO[14]
18	USER_GPIO[15]
19	P3.3V
20	P3.3V

X41 PIN.NO	NETNAME
1	EMC_AB[23]
2	SIGN525
3	
4	
5	
6	
7	
8	
9	
10	

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CONNECTOR TABLES
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X70 PIN.NO	A NETNAME	B NETNAME	C NETNAME	D NETNAME	E NETNAME	F NETNAME	G NETNAME	H NETNAME	J NETNAME	K NETNAME	L NETNAME	Y NETNAME
1	ERTEC_EMC	GND	EMC_DB[28]	EMC_DB[29]	ERTEC_EMC	GND	EMC_AB[6]	EMC_AB[9]	EMC_AB[12]	ERTEC_EMC	GND	ERTEC_EMC
2	GND	EMC_DB[26]	EMC_DB[27]	EMC_DB[31]	ERTEC_EMC	GND	EMC_AB[7]	EMC_AB[10]	EMC_AB[11]	EMC_AB[13]	EMC_AB[14]	GND
3	EMC_DB[24]	EMC_DB[25]	EMC_DB[30]	EMC_XBE3_DQM3	EMC_AB[5]	EMC_AB[8]	P3.3V_SEP	GND	EMC_XCS_SDRAM	EMC_XCAS_SDRAM	GND	EMC_DB[15]
4	EMC_DB[23]	EMC_DB[22]	EMC_DB[17]	EMC_DB[16]	EMC_AB[4]	EMC_AB[2]	EMC_AB[1]	EMC_AB[0]	EMC_XRAS_SDRAM	EMC_XWE_SDRAM	EMC_XRDY_BF	EMC_DB[0]
5	EMC_DB[21]	EMC_DB[19]	EMC_DB[20]	EMC_DB[18]	EMC_XBE2_DQM2	EMC_AB[3]	SIGN208	SIGN208	EMC_CLK_O_SDRAM1	EMC_XAV_BF	SIGN209	ERTEC_EMC
6	ERTEC_EMC	ERTEC_EMC	P1.5V_A_SEP	EMC_XCS_PER2	EMC_XCS_PER3	GND	EMC_XRDY_PER	ERTEC_EMC	EMC_CLK_O_SDRAM2	P3.3V_SEP	GND	GND
7	GND	GND	GND	GPIO[83]	GPIO[89]	GPIO[81]	GND	ERTEC_EMC	GND	P1.2V_SEP	P1.2V_SEP	P3.3V_SEP
8	SIGN542	SIGN543	P3.3V_SEP	GPIO[84]	GPIO[80]	ERTEC_PXHIF	ERTEC_PXHIF	GND	GND	P1.2V_SEP	P1.2V_SEP	SIGN364
9	P1_TDXN	P1_TDXP	SIGN363	GPIO[87]	GPIO[82]	SIGN307	GND	GND	GND	GND	GND	P2_TDXN
10	GND	SIGN11032	P1.5V_A_SEP	GPIO[88]	GPIO[91]	GND	P1.2V_SEP	P1.2V_SEP	GND	GND	GND	GND
11	P1_SDXN	P1_SDXP	GND	GPIO[86]	GPIO[94]	P3.3V_SEP	P1.2V_SEP	P1.2V_SEP	GND	GND	GND	P2_SDXN
12	P1_RDXN	P1_RDXP	P3.3V_SEP	GPIO[93]	GPIO[85]	GND	GND	GND	GND	GND	GND	P2_RDXN
13	GND	GND	GPIO[45]	GPIO[90]	GPIO[95]	ERTEC_PXHIF	ERTEC_PXHIF	GND	GND	P1.2V_SEP	P1.2V_SEP	GND
14	ERTEC_PXHIF	GPIO[39]	P1.5V_A_SEP	GPIO[92]	GPIO[62]	GPIO[63]	GND	ERTEC_PXHIF	GND	P1.2V_SEP	P1.2V_SEP	SIGN142
15	GPIO[48]	GPIO[44]	GPIO[33]	GPIO[36]	GPIO[35]	GND	GPIO[55]	ERTEC_PXHIF	SIGN307	GND	GPIO[54]	GND
16	GPIO[32]	GPIO[34]	GPIO[47]	GPIO[51]	GPIO[38]	GPIO[60]	GPIO[67]	GPIO[76]	GPIO[75]	GPIO[71]	GPIO[69]	P3.3V_SEP
17	GPIO[59]	GPIO[58]	GPIO[37]	GPIO[46]	GPIO[40]	GPIO[61]	GPIO[64]	GPIO[68]	GPIO[78]	GPIO[72]	GPIO[65]	GPIO[29]
18	ERTEC_PXHIF	GPIO[49]	GPIO[42]	GPIO[53]	GPIO[52]	P3.3V_SEP	SIGN11030	GND	GND	SIGN544	GND	GPIO[28]
19	GND	GPIO[41]	GPIO[43]	GPIO[50]	ERTEC_PXHIF	GND	P1.5V_A_SEP	P1_RXP	P1_TXP	SIGN214	GND	GND
20	ERTEC_PXHIF	GND	GPIO[57]	GPIO[56]	GND	P1.5V_A_SEP	SIGN11033	P1_RXN	P1_TXN	SIGN11033	SIGN11030	P3.3V_SEP

X70 PIN.NO	M NETNAME	N NETNAME	P NETNAME	R NETNAME	T NETNAME	U NETNAME	V NETNAME	W NETNAME
1	EMC_XRD	EMC_XWR	EMC_AB[19]	GND	ERTEC_EMC	EMC_DB[10]	EMC_DB[12]	GND
2	EMC_AB[16]	EMC_AB[17]	EMC_AB[20]	GND	ERTEC_EMC	EMC_DB[8]	EMC_DB[9]	EMC_DB[11]
3	P3.3V_SEP	P1.5V_A_SEP	ERTEC_TCK	EMC_AB[22]	EMC_XBE1_DQM1	EMC_DB[6]	EMC_DB[14]	EMC_DB[13]
4	EMC_AB[15]	EMC_AB[18]	ERTEC_XTRST	EMC_AB[23]	EMC_XCS_PER0	EMC_DB[5]	EMC_DB[1]	EMC_DB[3]
5	SIGN209	EMC_CLK_O_BF1	EMC_AB[21]	EMC_XCS_PER1	EMC_XBE0_DQM0	EMC_DB[7]	EMC_DB[2]	ERTEC_EMC
6	EMC_CLK_O_BF2	ERTEC_EMC	SIGN362	GND	SIGN11008	EMC_DTXR	EMC_DB[4]	GND
7	GND	ERTEC_EMC	GND	SIGN643	SIGN140	GPIO[1]	P1.5V_A_SEP	ERTEC_RTCK
8	GND	GND	P3.3V_SEP	P3.3V_SEP	ERTEC_TMS	GPIO[2]	GND	ERTEC_TDI
9	GND	GND	GND	SIGN312	GPIO[16]	GPIO[3]	GPIO[0]	P2_TDXP
10	GND	P1.2V_SEP	P1.2V_SEP	ERTEC_XSRST	GPIO[17]	GPIO[4]	SIGN541	SIGN11032
11	GND	P1.2V_SEP	P1.2V_SEP	GND	SIGN146	GPIO[5]	P1.5V_A_SEP	P2_SDXP
12	GND	GND	GND	SIGN309	P2_ACT	GPIO[6]	GND	P2_RDXP
13	GND	GND	P3.3V_SEP	P3.3V_SEP	P1_ACT	GPIO[7]	P1.5V_A_SEP	P3.3V_SEP
14	GND	ERTEC_PXHIF	GND	GND	GPIO[18]	GPIO[20]	GND	SIGN143
15	SIGN305	ERTEC_PXHIF	P3.3V_SEP	GND	GPIO[19]	GPIO[21]	SIG10007	ERTEC_XRST
16	GPIO[70]	GPIO[77]	GPIO[79]	GPIO[8]	GPIO[10]	GPIO[23]	GND	SIGN147
17	GPIO[73]	GPIO[74]	GPIO[66]	GPIO[9]	GPIO[11]	GPIO[13]	GPIO[15]	GPIO[26]
18	GND	GND	GND	GPIO[22]	GPIO[12]	GPIO[14]	GPIO[31]	GPIO[25]
19	P2_TXP	P2_RXP	P1.5V_A_SEP	GND	P3.3V_SEP	P2_LINK	GPIO[30]	GPIO[24]
20	P2_TXN	P2_RXN	SIGN11033	P1.5V_A_SEP	GND	P1_LINK	GPIO[27]	GND

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Sheet 36
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X81 PIN.NO	NETNAME
1	P3.3V
2	P5.0V
3	P3.3V
4	P5.0V
5	LS_XBE2_DQM2
6	LS_XBE3_DQM3
7	LS_XOE_DRIVER
8	LS_AB[15]
9	LS_DTXR
10	LS_AB[14]
11	LS_XRDY_PER
12	LS_AB[13]
13	LS_XRD
14	LS_AB[12]
15	LS_XWR
16	LS_AB[11]
17	LS_XCS_PER3
18	LS_AB[10]
19	LS_XCS_PER2
20	LS_AB[9]
21	LS_XCS_PER0
22	LS_AB[8]
23	LS_AB[23]
24	LS_AB[7]
25	LS_AB[22]
26	LS_AB[6]
27	LS_AB[21]
28	LS_AB[5]
29	LS_AB[20]
30	LS_AB[4]
31	LS_AB[19]
32	LS_AB[3]
33	LS_AB[18]
34	LS_AB[2]
35	LS_AB[17]
36	LS_AB[1]
37	LS_AB[16]
38	LS_AB[0]

X81 PIN.NO	SHIELDPINS NETNAME
S1	GND
S2	GND
S3	GND
S4	GND
S5	GND

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REFERENCE	TYPE	PIN_NO	
		AUX_P3.3V	GND
D29,D30	74LVC1G07	5	3

REFERENCE	TYPE	PIN_NO	
		GND	P12.0V
U1,U2	2901	12	3

REFERENCE	TYPE	PIN_NO					
		ERTEC_EMC	ERTEC_PXHIF	GND	P1.2V_SEP	P1.5V_A_SEP	P3.3V_SEP
D0	ERTEC200+	A1	A14	A10	G10	C10	C12
		A6	A18	A13	G11	C14	C8
		B6	A20	A19	H10	C6	F11
		E1	E19	A2	H11	G19	F18
		E2	F13	A7	K13	N3	G3
		H6	F8	B1	K14	P19	K6
		H7	G13	B13	K7	V11	M3
		K1	G8	B20	K8	V13	P13
		N6	H14	B7	L13	V7	P15
		N7	H15	C11	L14		P8
		T1	N14	C7	L7		R13
		T2	N15	E20	L8		R8
		W5		F1	N10		T19
		Y1		F10	N11		W13
		Y5		F15	P10		Y16
				F2	P11		Y20
				F6			Y7
				G12			
				G14			
				G7			
				G9			
				H12			
				H13			
				H3			
				H8			
				H9			
				J10			

REFERENCE	TYPE	PIN_NO	
		ERTEC_EMC	GND
D18,D19	SDRAM 32Mx16	A7	A1
		A9	A3
		B3	B7
		C7	C3
		D3	D7
		E7	E3
		J9	J1
D22,D23	S29WS128P	B6	B3
		J5	G3
		L5	J9
		L8	L4
D44	74LVC1G157	5	2

REFERENCE	TYPE	PIN_NO					
		ERTEC_EMC	ERTEC_PXHIF	GND	P1.2V_SEP	P1.5V_A_SEP	P3.3V_SEP
D0	ERTEC200+			J11			
				J12			
				J13			
				J14			
				J7			
				J8			
				J9			
				K10			
				K11			
				K12			
				K15			
				K9			
				L1			
				L10			
				L11			
				L12			
				L18			
				L3			
				L6			
				L9			
				M10			
				M11			
				M12			
				M13			
				M14			
				M7			
				M8			
				M9			
				N12			
				N13			
				N8			
				N9			
				P12			
				P14			
				P18			
				P7			
				P9			
				R1			
				R11			
				R15			
				R2			
				R6			
				T20			
				V12			
				V16			
				V8			
				W1			
				W20			
				W6			
				Y10			
				Y13			
				Y15			
				Y19			
				Y2			
				Y6			

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REFERENCE	TYPE	PIN_NO		
		ERTEC_EMC	GND	P3.3V
D14,D15,D16,D17	74LVC16T245	31 42	10 15 21 28 34 39 4 45	18 7
D40,D41,D42	74LVC2T45	1	4	8

REFERENCE	TYPE	PIN_NO	
		GND	P3.3V
D2,D3	74ALVC16244	10 15 21 28 34 39 4 45	18 31 42 7
D5	24C16	4	8
D7	SN65HVD10	5	8
D13	24C256	4	8
D27	serialFlash_16Mb	4	8
D28,D32,D33,D34 D35,D36,D37 D38,D39,D43	74LVC1G07	3	5

REFERENCE	TYPE	PIN_NO		
		GND	P3.3V	USB_P1.8V
D12	TUSB3410	18 28 8	25 3	4

REFERENCE	TYPE	PIN_NO	
		GND	POF_SD_P3.3V
D45	100LVELT22	5	8
U4	TLV3502	5	8

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Group Spacings for External Layers

	EARTH	NoGroup	DiffPair	ExtPWR
EARTH	0.50	0.50	0.50	0.50
NoGroup	0.50	B-ISO	B-ISO	0.50
DiffPair	0.50	B-ISO	B-ISO	0.50
ExtPWR	0.50	0.50	0.50	0.50

Group Spacings for Internal Layers

	EARTH	NoGroup	DiffPair	ExtPWR
EARTH	0.50	0.50	0.50	0.50
NoGroup	0.50	B-ISO	B-ISO	0.50
DiffPair	0.50	B-ISO	B-ISO	0.50
ExtPWR	0.50	0.50	0.50	0.50

Not Connected Pin Table

EPL	PIN.NO	Spacing Class
D1	A10	NoGroup
D1	A13	NoGroup
D1	A4	NoGroup
D1	A5	NoGroup
D1	A6	NoGroup
D1	A7	NoGroup
D1	A8	NoGroup
D1	B10	NoGroup
D1	B13	NoGroup
D1	B3	NoGroup
D1	B4	NoGroup
D1	B5	NoGroup
D1	B7	NoGroup
D1	B8	NoGroup
D1	C10	NoGroup
D1	C13	NoGroup
D1	C5	NoGroup
D1	C8	NoGroup
D1	D10	NoGroup
D1	D11	NoGroup
D1	D12	NoGroup
D1	D13	NoGroup
D1	D14	NoGroup
D1	D4	NoGroup
D1	D5	NoGroup
D1	D6	NoGroup
D1	D7	NoGroup
D1	E11	NoGroup
D1	E6	NoGroup
D1	E8	NoGroup
D1	E9	NoGroup
D1	F10	NoGroup

Not Connected Pin Table

EPL	PIN.NO	Spacing Class
X1	A7	NoGroup
X1	B7	NoGroup
X1	C10	NoGroup
X1	C11	NoGroup
X1	C12	NoGroup
X1	C7	NoGroup
X1	C9	NoGroup
X1	D10	NoGroup
X1	D11	NoGroup
X1	D12	NoGroup
X1	D7	NoGroup
X1	D9	NoGroup
X11	4	NoGroup
X2	COP1	NoGroup
X2	COP2	NoGroup
X20	6	NoGroup
X21	6	NoGroup
X22	5	NoGroup
X22	6	NoGroup
X3	COP1	NoGroup
X3	COP2	NoGroup
X30	1	NoGroup
X30	10	NoGroup
X30	2	NoGroup
X30	3	NoGroup
X30	4	NoGroup
X30	5	NoGroup
X4	COP1	NoGroup
X4	COP2	NoGroup
X41	10	NoGroup
X41	3	NoGroup
X41	4	NoGroup
X41	5	NoGroup
X41	6	NoGroup
X41	7	NoGroup
X41	8	NoGroup
X41	9	NoGroup
X43	10	NoGroup
X43	3	NoGroup
X43	4	NoGroup
X43	5	NoGroup
X43	6	NoGroup
X43	7	NoGroup
X43	8	NoGroup
X43	9	NoGroup
X60	A5	NoGroup
X60	A6	NoGroup
X60	A7	NoGroup
X60	A8	NoGroup
X60	B11	NoGroup
X60	B12	NoGroup
X60	B3	NoGroup
X60	B5	NoGroup
X60	B6	NoGroup
X60	B9	NoGroup

Not Connected Pin Table

EPL	PIN.NO	Spacing Class
D23	H9	NoGroup
D23	J2	NoGroup
D23	J6	NoGroup
D23	K2	NoGroup
D23	K6	NoGroup
D23	K9	NoGroup
D23	L2	NoGroup
D23	L3	NoGroup
D23	L6	NoGroup
D23	L7	NoGroup
D23	L9	NoGroup
D23	M1	NoGroup
D23	M10	NoGroup
D28	1	NoGroup
D29	1	NoGroup
D3	11	NoGroup
D3	12	NoGroup
D3	6	NoGroup
D3	8	NoGroup
D3	9	NoGroup
D30	1	NoGroup
D32	1	NoGroup
D33	1	NoGroup
D34	1	NoGroup
D35	1	NoGroup
D36	1	NoGroup
D37	1	NoGroup
D38	1	NoGroup
D39	1	NoGroup
D4	10	NoGroup
D4	19	NoGroup
D4	20	NoGroup
D4	23	NoGroup
D4	9	NoGroup
D42	3	NoGroup
D43	1	NoGroup
D6	10	NoGroup
D9	16	NoGroup
D9	19	NoGroup
D9	20	NoGroup
D9	23	NoGroup
N1	7	NoGroup
N10	7	NoGroup
N10	8	NoGroup
N12	6	NoGroup
N2	7	NoGroup
N3	2	NoGroup
N9	7	NoGroup
N9	8	NoGroup
R440	8	NoGroup
U1	13	NoGroup
U1	14	NoGroup
U3	2	NoGroup
V2	NC	NoGroup
V3	NC	NoGroup

Not Connected Pin Table

EPL	PIN.NO	Spacing Class
D1	F7	NoGroup
D1	F8	NoGroup
D1	F9	NoGroup
D1	K13	NoGroup
D11	20	NoGroup
D11	23	NoGroup
D12	2	NoGroup
D12	21	NoGroup
D12	22	NoGroup
D12	29	NoGroup
D12	30	NoGroup
D12	31	NoGroup
D12	32	NoGroup
D18	E2	NoGroup
D19	E2	NoGroup
D22	A1	NoGroup
D22	A10	NoGroup
D22	B5	NoGroup
D22	B7	NoGroup
D22	B8	NoGroup
D22	B9	NoGroup
D22	C4	NoGroup
D22	C9	NoGroup
D22	D4	NoGroup
D22	D6	NoGroup
D22	F5	NoGroup
D22	G5	NoGroup
D22	G6	NoGroup
D22	H9	NoGroup
D22	J2	NoGroup
D22	J6	NoGroup
D22	K2	NoGroup
D22	K6	NoGroup
D22	K9	NoGroup
D22	L2	NoGroup
D22	L3	NoGroup
D22	L6	NoGroup
D22	L7	NoGroup
D22	L9	NoGroup
D22	M1	NoGroup
D22	M10	NoGroup
D23	A1	NoGroup
D23	A10	NoGroup
D23	B5	NoGroup
D23	B7	NoGroup
D23	B8	NoGroup
D23	B9	NoGroup
D23	C4	NoGroup
D23	C9	NoGroup
D23	D4	NoGroup
D23	D6	NoGroup
D23	E5	NoGroup
D23	F5	NoGroup
D23	G5	NoGroup
D23	G6	NoGroup

updateDate=13/02/05
updateTime=07:44:25

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SPACING CLASSES
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