New IGBT-PIM with 6th Generation Chip and Package Technologies

Hayato Nakano
Yuichi Onozawa
Osamu Ikawa

1. Introduction

Power electronics, typically used for power control and conversion, have been utilized in a rapidly expanding range of applications in recent years. The main marketplace requirements for the latest power conversion system are small size, light weight and high efficiency. Therefore, technological improvements to power semiconductors are needed in order to achieve higher performance, more advanced functions and higher power handling capability.

One solution for system downsizing is to utilize an IGBT-PIM (power integrated module), in which an inverter circuit, a dynamic brake circuit and a rectifier diode are integrated all together in one module. The demand for PIMs has been increasing for several years because of their advantages of size and easy assembly, and because they provide an economical solution.

The next generation PIMs should have much smaller sizes and more economical features. The key to achieving high-performance compact PIMs is technology for reducing the silicon area while managing the electrical and thermal performance. The IGBT chip is undoubtedly the most important component in a PIM, and as such, must be designed with special consideration to exhibit the best performance. Because IGBT chips are the largest components and have the highest temperature in a module, a thermal management solution is always required. The development of both chip and packaging technologies is important for realizing high-performance compact PIMs, i.e., IGBTs should have be provided with improved power dissipation in a package having lower thermal impedance.

Another feature that new PIMs must exhibit is low noise radiation. The switching power dissipation can be classified as "static" and "dynamic" power dissipation. Static dissipation, which is related to the on-state voltage drop (V_{on}), depends slightly on the duty cycle, but is not strongly dependant on the driving condition. Dynamic dissipation, however, which integrates turn-on and turn-off energy, is significantly related to the driving condition.

2. New IGBT Chip Design Consideration

2.1 Performance challenges

The field stop structure, shown in Fig. 1, makes it possible to reduce the device thickness dramatically, which results in a significant performance improvement[1]. However, the turn-off oscillation issue that was observed in the Epi-type IGBT of the early 1990's has again become a potential problem. When the device becomes thin, it is easy to have "depletion layer reach-through" to the field-stop layer, which is the mechanism of the turn-off oscillation. The critical voltage of the oscillation should be outside of the SOA.

Thus, a breakthrough in the trade-off between the critical oscillation voltage and the breakdown voltage is needed in order to reduce device thickness. The critical voltage increases with lower-resistivity silicon, however the breakdown voltage decreases simultaneously.

The "ideal factor", shown in Fig. 2, is an important tool for understanding these criteria. The "ideal factor" is the ratio between the breakdown voltage of a real device and that of a theoretical plane junction with the same bulk resistivity and thickness. A 140 µm-thick FS-IGBT can be designed to only 70% of the ideal factor in order to obtain oscillation-free turn-off, however, a 120 µm-thick device can achieve at least 86% of the ideal factor without oscillation.

2.2 Easy *dv/dt* control

It is well known that an FWD having soft reverse recovery behavior is important for achieving lower turn-on dv/dt. However, there is little published work to report the importance of IGBT turn-on characteristics.

The planar gate-IGBT, which has enjoyed great popularity in the 20th century, has simple gate structures, and therefore its dynamic behavior is easy to predict based on physical dimensions. Trench IGBTs, however, have more variations and complexity in their gate structure, layout, and in optimization methods to compensate low V_{on} and provide a specific short-circuit capability.

Figure 3 shows an example of turn-on di/dt and dv/dt controllability with various gate resistances for

Fig.1 Cross-sectional view of each generation of 1,200 V IGBT chips

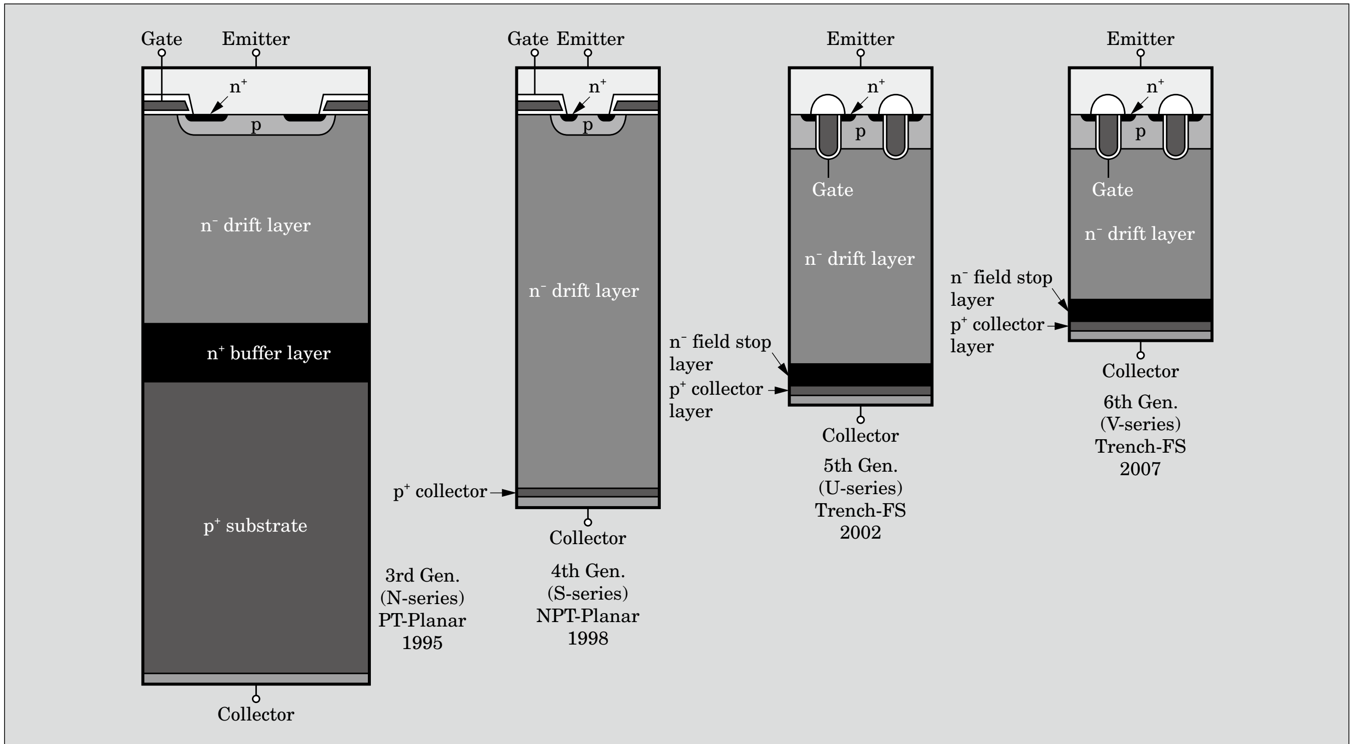


Fig.2 "Ideal factor" required for oscillation-free turn-off FS-IGBT as a function of the device thickness

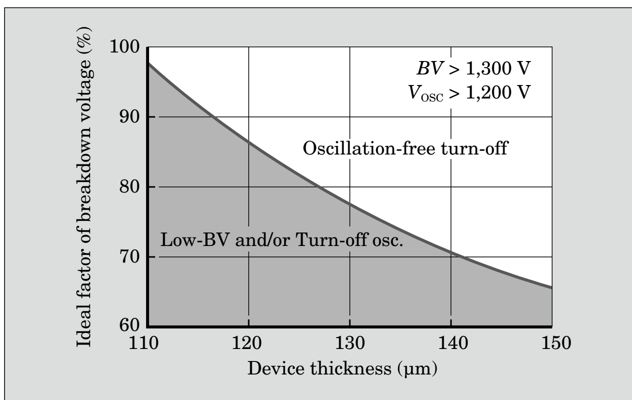
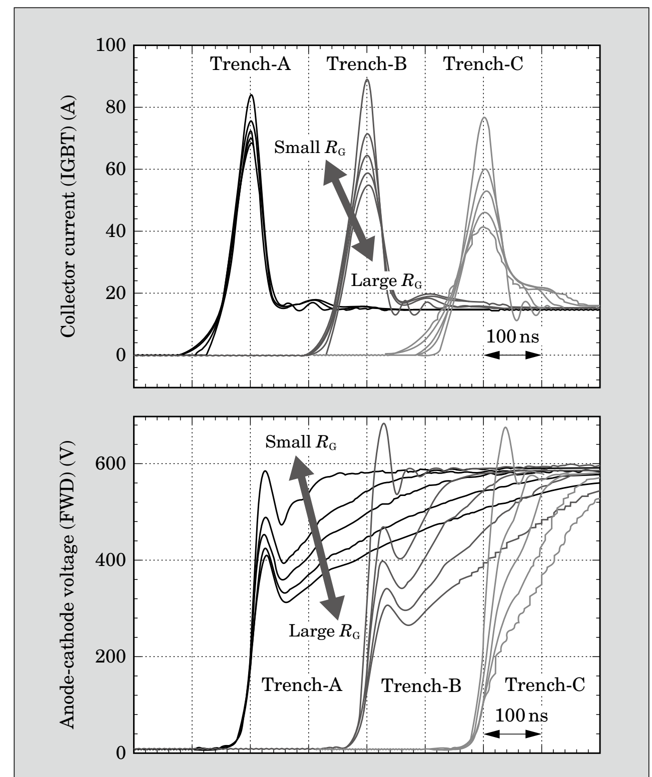


Fig.3 Small current turn-on dv/dt controllability with R_G for trench IGBTs with different gate designs



different trench gate designs. The turn-on current was 15 A, which is 1/5 of the rated current of 75 A. The gate resistance was varied from 7.7 Ω to 40 Ω. The FWD and IGBT were assembled separately on a special test piece to obtain only the effect of the IGBT design for the same FWD.

It is obvious that the turn-on behavior strongly depends on the trench design. Trench-A exhibits very little change in the switching waveforms versus gate resistance. Thus it is difficult to control dv/dt and di/dt with the gate resistance of this device. On the other hand, Trench-C shows outstanding controllability. The peak collector current, di_C/dt and dv_{AK}/dt can easily be controlled simply with a change in the gate resistance.

Hard switching behavior is often considered to be caused by a poor design for FWDs. This is obviously correct, and hard reverse recovery FWDs are difficult to use with the new IGBT modules. However, in case of a trench-gate IGBT, it should be noted that turn-on be-

havior would be another cause of hard switching even though the FWDs are designed to have a soft recovery feature[(2)].

V-IGBT optimizations have been carried out with the following key goals[(3)].

(1) To realize a high "ideal factor" for both the main structure and junction termination
(2) To reduce the device thickness as much as possible while maintaining the oscillation-free turn-off performance
(3) To adjust the short-circuit current to have a consistent value and to maintain 10 µs-capability even at 150 °C
(4) To reduce the gate capacitance to the extent possible for fast switching
(5) To obtain consistent ruggedness and long-term reliability

3. Experimental Results

3.1 Static characteristics

After the device design was optimized, a 1,200 V-75 A V-IGBT and FWD chipset was experimentally evaluated. Figure 4 shows the J-V characteristics at room temperature and 125 °C, respectively, with a comparison to the current generation U-IGBT die. In order to make sure the improvement compared to the conventional device, the Y-axis is represented by current density. At a collector current density of 115 A/cm^2, a V_{on} of 1.7 V for the V-IGBT and 2.2 V for the U-IGBT, a reduction in V_{on} of up to 0.5 V has been achieved by optimizing the device structure and reducing the device thickness.

This great improvement in V_{on} clearly indicates the possibility of an increase in the rated current density while maintaining a lower V_{on} than in conventional devices.

3.2 Switching performance

Figure 5 shows a demonstration representing the improvement in the turn-off oscillation feature of a V-IGBT. The measurement conditions were: V_{DC} = 1,250 V, I_C = 150 A, V_{GE} = +15 V, −15 V and T_j = 150 °C. The figures clearly show that the V-IGBT has soft turn-off behavior with no oscillation even at extreme conditions. As a result of many measurements of turn-off oscillation at various ranges of DC-link voltage and temperature, it has been confirmed that no oscillation was found within the SOA guarantee.

Fig.4 J-V characteristics of a V-series IGBT

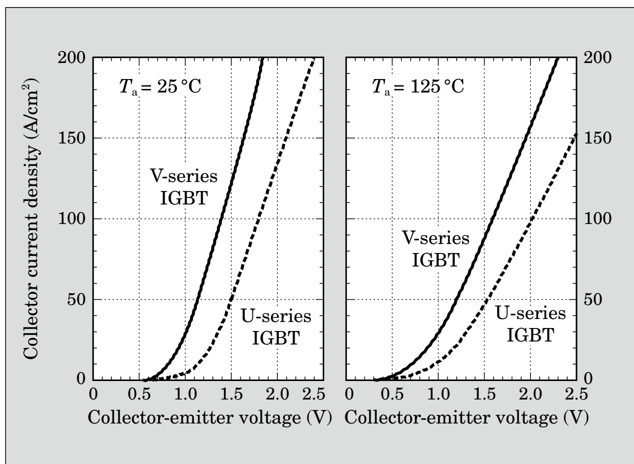


Fig.5 Extreme measurement results demonstrating the turn-off oscillation V_{DC} = 1,250 V, I_C = 150 A

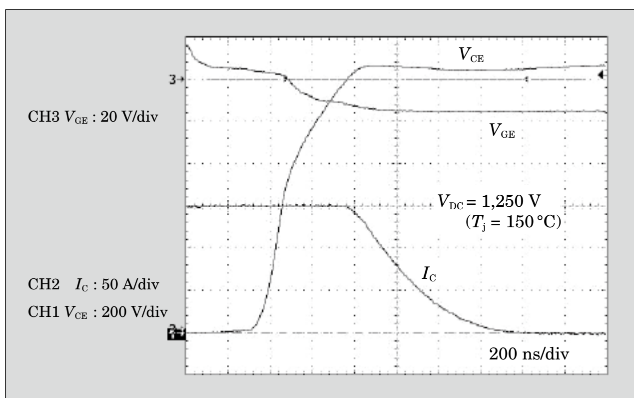
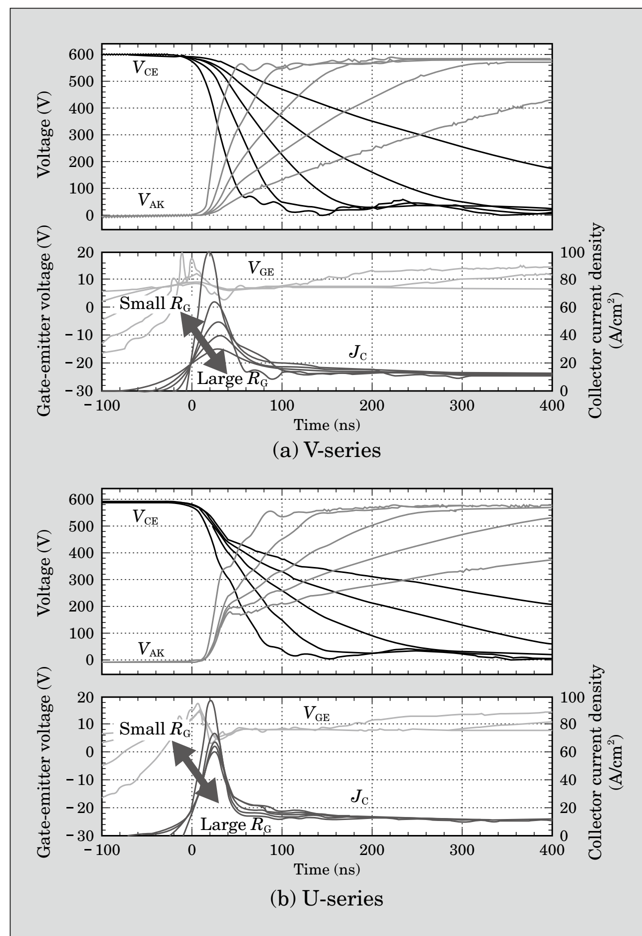


Fig.6 Comparison of small current turn-on behavior for different gate resistances



creasing R_G, V-IGBT will meet the target much faster than other IGBTs. This means fewer penalties in terms of switching loss in practical applications.

3.3 The "noise vs. switching loss" trade-off

The experimental results of the small current turn-on behavior of V-IGBTs and conventional IGBTs with various gate resistances are shown in Fig. 6. The measurement conditions were: V_{CE} = 600 V, J_C = 11.7 A/cm^2, V_{GE} = +15 V to −15 V and T_j = R.T.

As mentioned earlier, the FWD dv_{AK}/dt corresponds to the IGBT turn-on di_C/dt. This means that with a new IGBT having excellent turn-on di_C/dt sensitivity to the gate resistance, control is much easier to implement in the FWD dv_{AK}/dt optimization process to compensate for noise radiation.

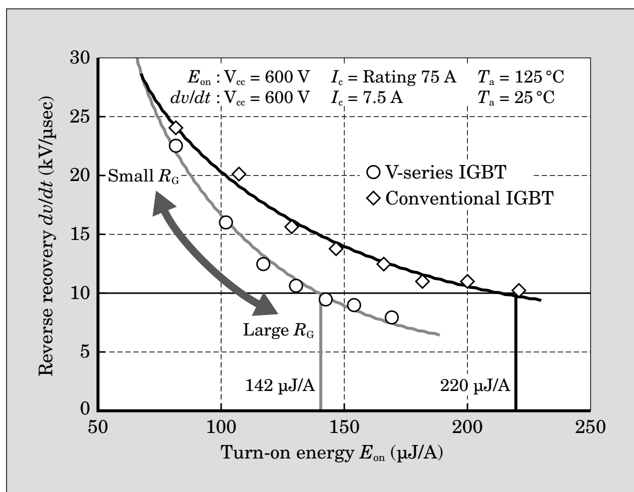
In addition, it is obvious from the figure that the V_{CE} waveforms strongly depend on the gate resistance. The higher the gate resistance is, the longer the voltage tail that appears in V_{CE} waveforms. These V_{CE} waveforms are observed not only for small current turn-on, but over the entire current range. Therefore, using an IGBT with poor di_C/dt controllability results in a greater penalty in E_{on}, in order to reduce noise.

Figure 7 shows the trade-off relationship between the FWD $dv_{AK}/dt_{(max)}$ at a small current (1/10 of rated current) and the IGBT E_{on} at a large current (rated current). The gate resistances were varied in the measurements. The measurement method used is the same as was used to create Fig. 3. The same FWD test piece was employed to isolate only the differences in the IGBT structure.

In case of the conventional IGBT, the turn-on energy of the large current is 220 µJ/A when the gate resistance is adjusted to the target dv_{AK}/dt at the small current turn-on of 10 kV/µs. On the other hand, the new large current IGBT has lower dv/dt characteristics over the entire range, and E_{on} at large current operation is a much lower value of 142 µJ/A, which is about a 36% smaller E_{on}.

When measurements are started with a smaller gate resistance to find the target dv/dt by slightly in-

Fig.7 Trade-off between small current $dv/dt_{(max)}$ and turn-on energy at rated current



3.4 Ruggedness

One of the key features of the trench-FS IGBT is its high-temperature short-circuit capability. Figure 8 (a) shows the short-circuit measurement of V-IGBTs. Short-circuit gate pulses of +15 V, 10 µs width were applied to the gate at V_{DC} = 800 V and T_j = 150 °C. The device successfully turned off, because the V-IGBT has been designed during the device optimization stage to have a consistent short-circuit current.

Figure 8 (b) is an extreme demonstration of the device's ruggedness. The short-circuit measurement was performed with an intentionally large main inductance at 150 °C and a +15 V gate pulse of 8 µs width. No soft turn-off method was applied. The device survived the most critical condition of the self-clamping mode. This test also confirms that V-IGBTs have large switching current self-clamping capability.

3.5 Total power and temperature increase

It should be noted that it is very important to consider the rated current density of the new IGBTs while determining an optimum balance in terms of thermal management. In general, the smaller the silicon die size is, the higher the thermal impedance will be, and therefore, it is necessary to also achieve lower thermal impedance packaging technologies and combine them

Fig.8 Short-circuit demonstration of V-series IGBT at 150 °C

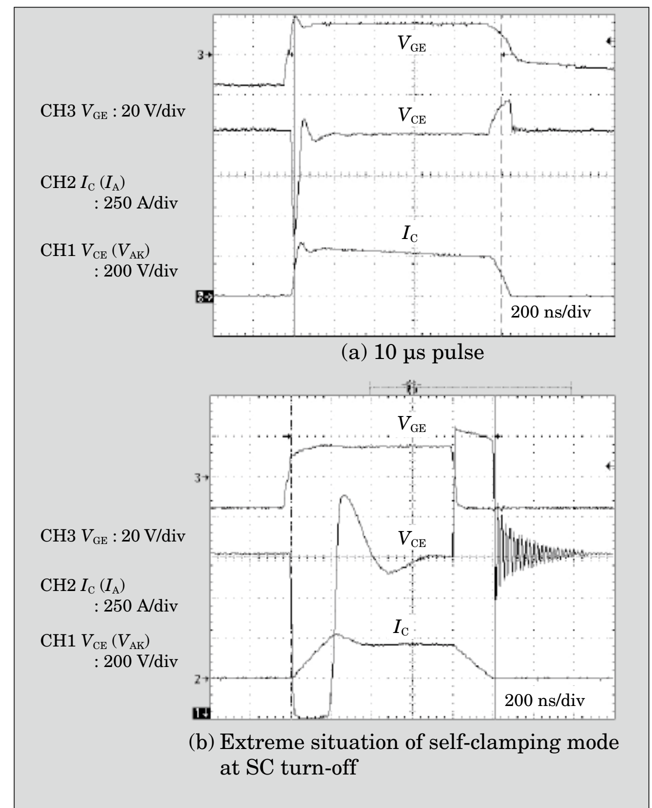


Fig.9 Estimated total power and ΔT_{j-c} with adjusted R_G to obtain similar noise peaks

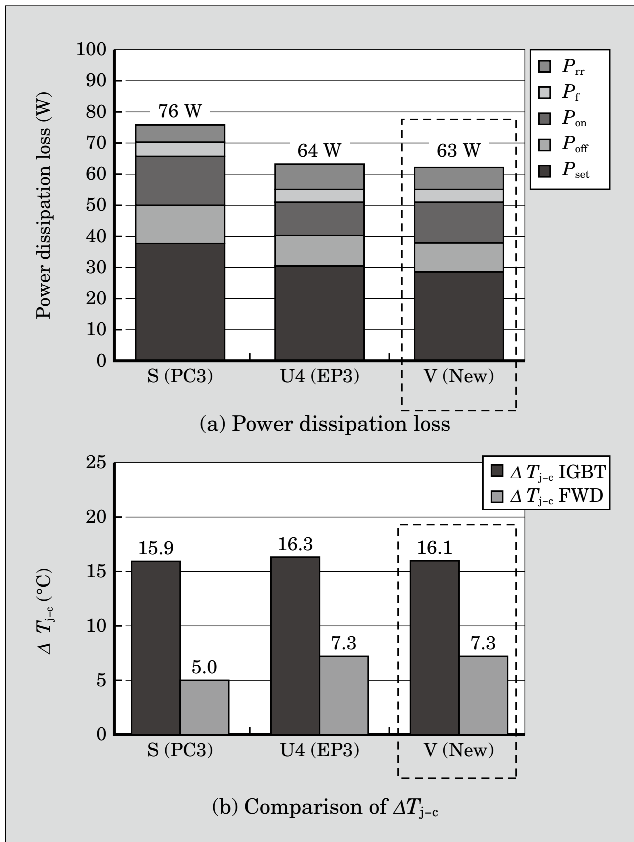
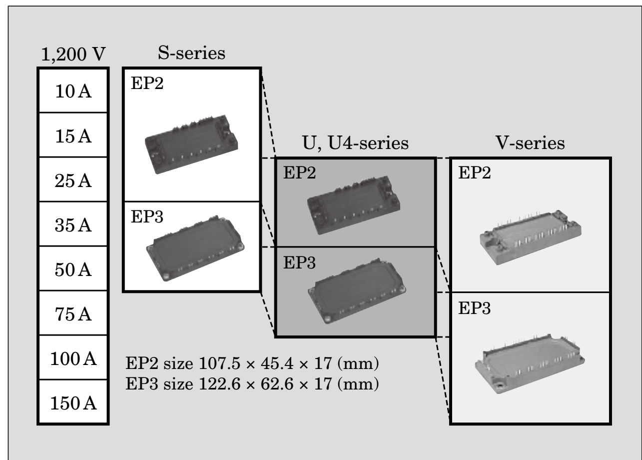


Fig.10 Product current rating by module size of Fuji's IGBT-PIMs



with techniques for shrinking the silicon die.

Figure 9 shows the estimated power dissipation and ΔT_j in a typical overdrive condition of a motor application. The gate resistances were experimentally selected so that these chip sets had similar FWD dv/dt at low current turn-on. It is clear from the figure that the total power dissipation of the V-series is 63 W, which is very similar to the 64 W power dissipation of the U4-series. An estimate of the temperature rise is also available, as shown in Fig. 9 (b). The ΔT_{j-c} of the IGBT is 16.1 °C for the V-series, which is very similar to that of former generation modules.

4. Product Line-up

Compared to the S-series and U4-series, V-series PIMs have a smaller IGBT die size. The impact of these results is directly apparent in the enhancement of the module power capacity. Figure 10 shows the 1,200 V PIM line-up listed by module type and rated current. The new product will have the same footprint size as the EP2 package up to 1,200 V-50 A. For the EP3-compatible physical size, a significant increase in current range has been achieved. 1,200 V PIMs of 100 A and 150 A rated current are available with the Fuji V-series of IGBT PIMs.

5. Postscript

Fuji V-series IGBT PIMs have been presented in this paper. The 6th generation chip has made it possible to realize IGBT PIMs having "low noise radiation," "compact size" and "high performance." The PIM power range has been extended up to 1,200 V-150 A with an EP3-compatible size package. Fuji's new PIMs are helping to provide more effective and economical solutions of power electronics.

References

(1) Laska. T. et al. The Field Stop IGBT (FS IGBT) – A new power device concept with a great improvement potential. Proc. ISPSD 2000. p.355-358.

(2) Nemoto. M. et al. An Advanced FWD Design Concept with Superior Soft Reverse Recovery Characteristics. Proc. ISPSD 2000. p.119-122.

(3) Otsuki. M. et al. Investigation on the short-circuit capability of 1,200V trench gate field-stop IGBTs. Proc. ISPSD 2002. p.281-284.

＊ All brand names and product names in this journal might be trademarks
or registered trademarks of their respective companies.