

FMV60N160S2HF

Super J MOS[®] S2 series

N-Channel enhancement mode power MOSFET

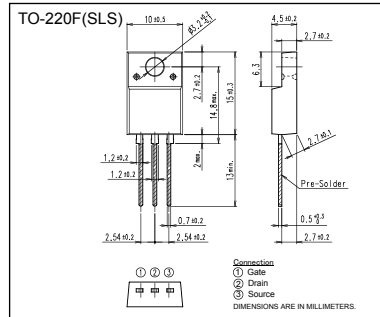
Features

- Pb-free lead terminal
- RoHS compliant
- uses Halogen-free molding compound

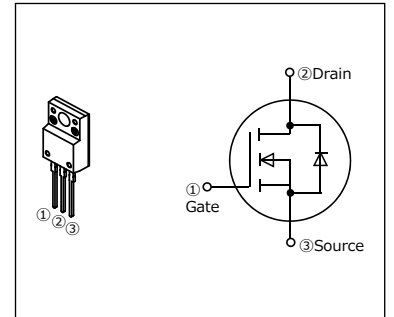
Applications

- For switching

Outline Drawings [mm]



Equivalent circuit schematic



Absolute Maximum Ratings at $T_c=25^\circ\text{C}$ (unless otherwise specified)

| Parameter | Symbol | Characteristics | Unit | Remarks |
|--|--------------|-----------------|------------------|----------------------------------|
| Drain-Source Voltage | V_{DS} | 600 | V | |
| | V_{DSX} | 600 | V | $V_{GS}=-30V$ |
| Continuous Drain Current | I_D | 23.9 | A | $T_c=25^\circ\text{C}$ Note*1,2 |
| | | 15.1 | A | $T_c=100^\circ\text{C}$ Note*1,2 |
| Pulsed Drain Current | I_{DP} | 71.6 | A | Note *2 |
| Gate-Source Voltage | V_{GS} | ± 30 | V | |
| Non-Repetitive Maximum Avalanche Current | I_{AS} | 2.7 | A | Note *3 |
| Non-Repetitive Maximum Avalanche Energy | E_{AS} | 618 | mJ | Note *4 |
| Maximum Drain-Source dV/dt | dV_{DS}/dt | 50 | V/ns | $V_{DS} \leq 600V$ |
| Continuous Diode Forward Current | I_{SD} | 23.9 | A | $T_c=25^\circ\text{C}$ Note*1,2 |
| | | 15.1 | A | $T_c=100^\circ\text{C}$ Note*1,2 |
| Pulsed Diode Forward Current | I_{SDP} | 71.6 | A | Note *2 |
| Peak Diode Recovery dV/dt | dV/dt | 15 | V/ns | Note *5 |
| Peak Diode Recovery -di/dt | $-di/dt$ | 100 | A/ μs | Note *6 |
| Maximum Power Dissipation | P_D | 2.16 | W | $T_a=25^\circ\text{C}$ |
| | | 45 | | $T_c=25^\circ\text{C}$ |
| Operating and Storage Temperature range | T_{ch} | 150 | $^\circ\text{C}$ | |
| | T_{stg} | -55 to +150 | $^\circ\text{C}$ | |
| Isolation Voltage (TO-220F) | V_{iso} | 2 | kVrms | $t=60\text{sec}, f=60\text{Hz}$ |

Note *1 : Maximum duty cycle $D=0.65$
 Note *2 : Limited by maximum channel temperature.
 Note *3 : $T_{ch} \leq 150^\circ\text{C}$, See Fig.1 and Fig.2
 Note *4 : Starting $T_{ch}=25^\circ\text{C}$, $I_{AS}=1.7A$, $L=392\text{mH}$, $V_{DD}=60V$, $R_G=50\Omega$, See Fig.1 and Fig.2
 E_{AS} limited by maximum channel temperature and avalanche current.
 Note *5 : $I_{SD} \leq 17.9A$, $-di/dt \leq 100A/\mu\text{s}$, $V_{DS \text{ peak}} \leq 600V$, $T_{ch} \leq 150^\circ\text{C}$.
 Note *6 : $I_{SD} \leq 17.9A$, $dV/dt \leq 15V/ns$, $V_{DS \text{ peak}} \leq 600V$, $T_{ch} \leq 150^\circ\text{C}$.

■ Electrical Characteristics at $T_c=25^\circ\text{C}$ (unless otherwise specified)

• Static Ratings

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|----------------------------------|--------------|--|------|-------|-------|----------|
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V$ $I_D=250\mu A$ | 600 | - | - | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}$ $I_D=0.95mA$ | 3.5 | 4.0 | 4.5 | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=600V$ $V_{GS}=0V$ $T_{ch}=25^\circ\text{C}$ | - | - | 25 | μA |
| | | $V_{DS}=480V$ $V_{GS}=0V$ $T_{ch}=125^\circ\text{C}$ | - | - | 250 | |
| Gate-Source Leakage Current | I_{GSS} | $V_{DS}=0V$ $V_{GS}=\pm 30V$ | - | 10 | 100 | nA |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}=10V$ $I_D=9.0A$ | - | 0.146 | 0.160 | Ω |
| Gate resistance | R_G | f=1MHz, open drain | - | 9.8 | - | Ω |

• Dynamic Ratings

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|--------------|---|------|------|------|---------|
| Forward Transconductance | g_{fs} | $V_{DS}=25V$ $I_D=9.0A$ | 5.7 | 11.5 | - | S |
| Input Capacitance | C_{iss} | $V_{DS}=400V$ $V_{GS}=0V$ f=250kHz | - | 990 | - | μF |
| Output Capacitance | C_{oss} | | - | 35 | - | |
| Reverse Transfer Capacitance | C_{rss} | | - | 5.3 | - | |
| Effective output capacitance, energy related (Note *7) | $C_{o(er)}$ | $V_{DS}=0\dots 400V$ $V_{GS}=0V$ | - | 83 | - | μF |
| Effective output capacitance, time related (Note *8) | $C_{o(tr)}$ | $V_{DS}=0\dots 400V$ $V_{GS}=0V$ $I_D=\text{constant}$ | - | 308 | - | μF |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}=400V, V_{GS}=10V$ $I_D=9.0A,$ $R_G=15\Omega$ See Fig.3 and Fig.4 | - | 19 | - | ns |
| | t_r | | - | 63 | - | |
| Turn-Off Time | $t_{d(off)}$ | | - | 87 | - | |
| | t_f | | - | 23 | - | |
| Total Gate Charge | Q_G | $V_{DD}=400V, V_{GS}=10V$ $I_D=17.9A$ See Fig.5 | - | 43 | - | nC |
| Gate-Source Charge | Q_{GS} | | - | 17 | - | |
| Gate-Drain Charge | Q_{GD} | | - | 16 | - | |
| Drain-Source crossover Charge | Q_{SW} | | - | 11 | - | |

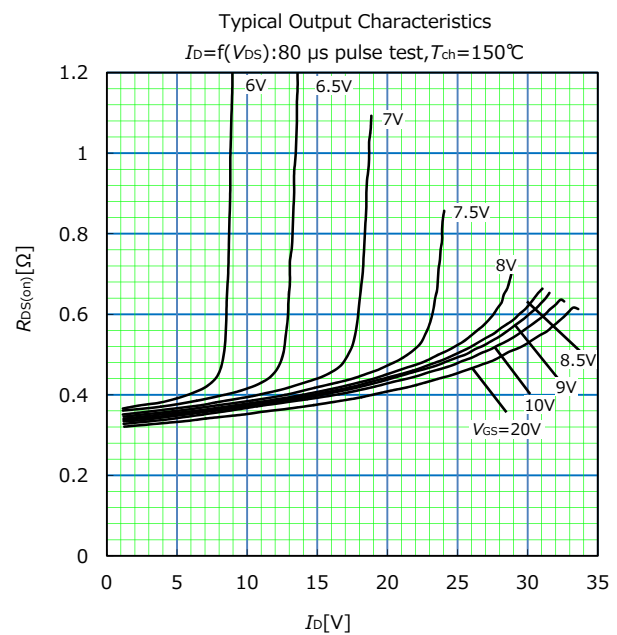
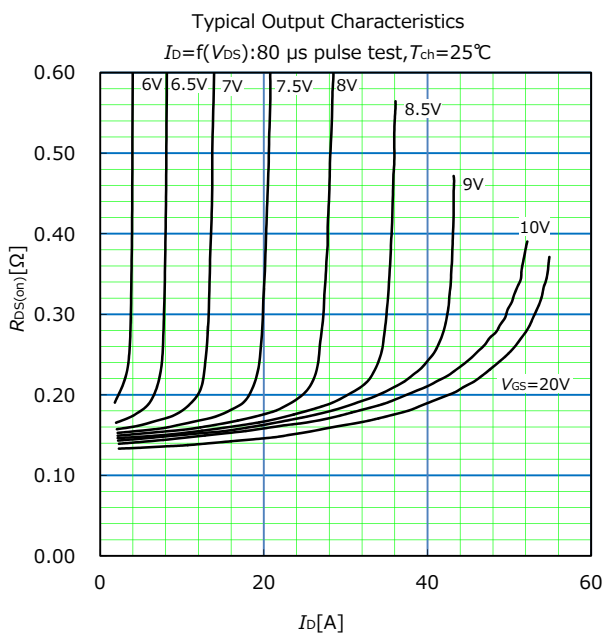
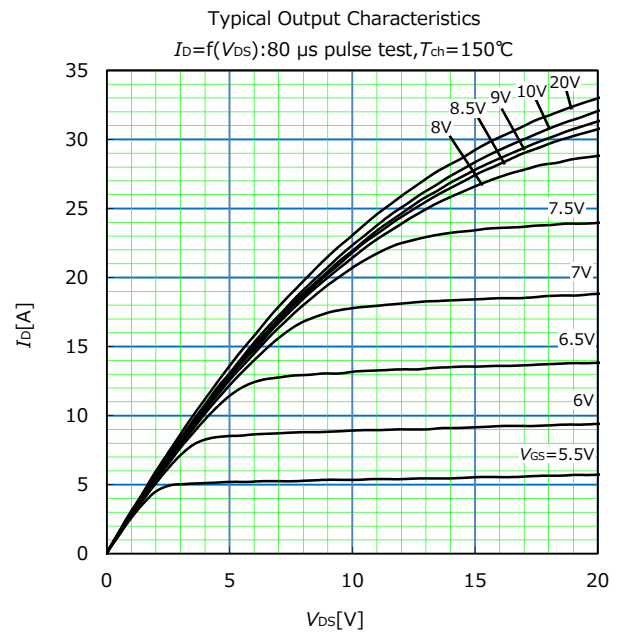
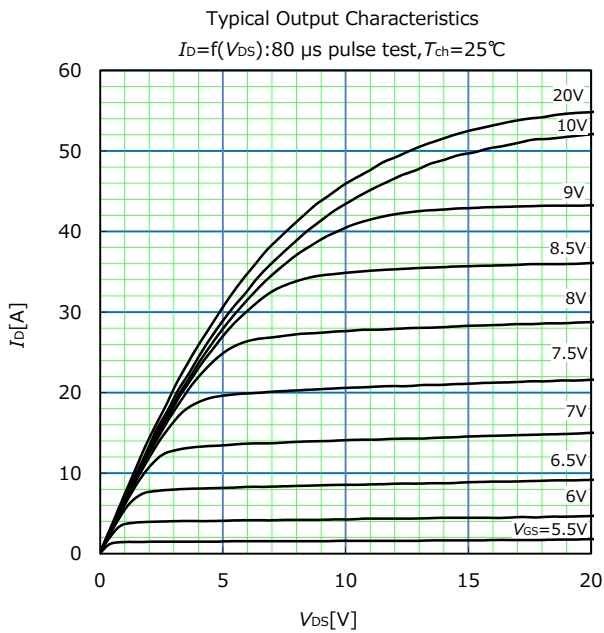
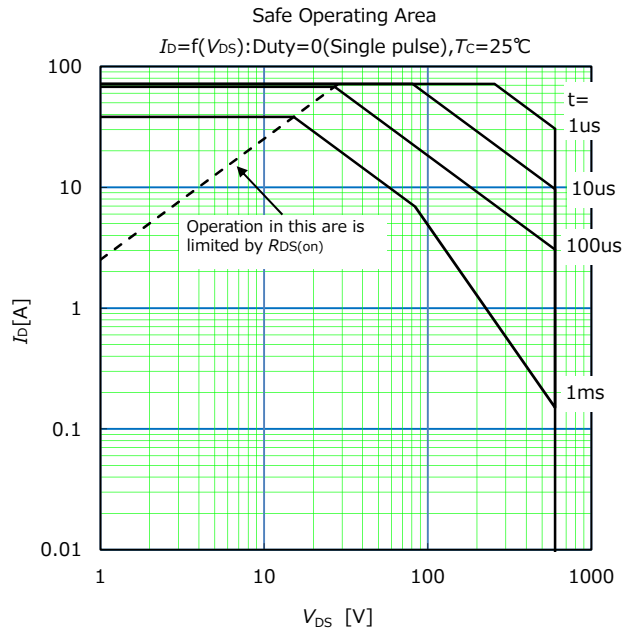
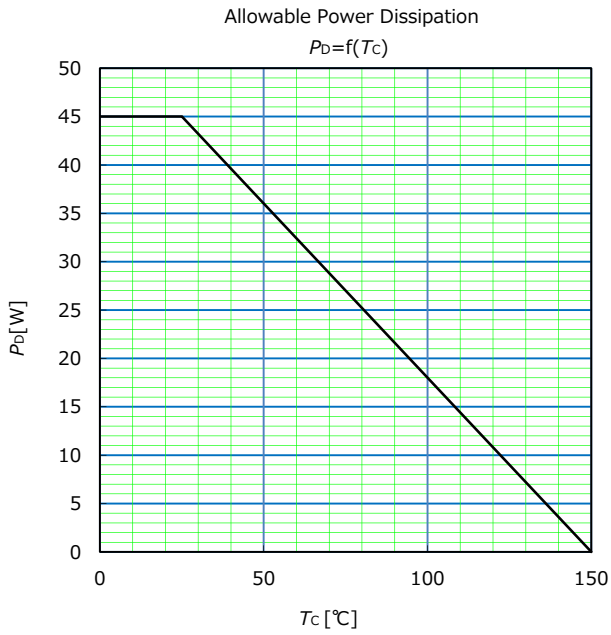
Note *7 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
 Note *8 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 400V.

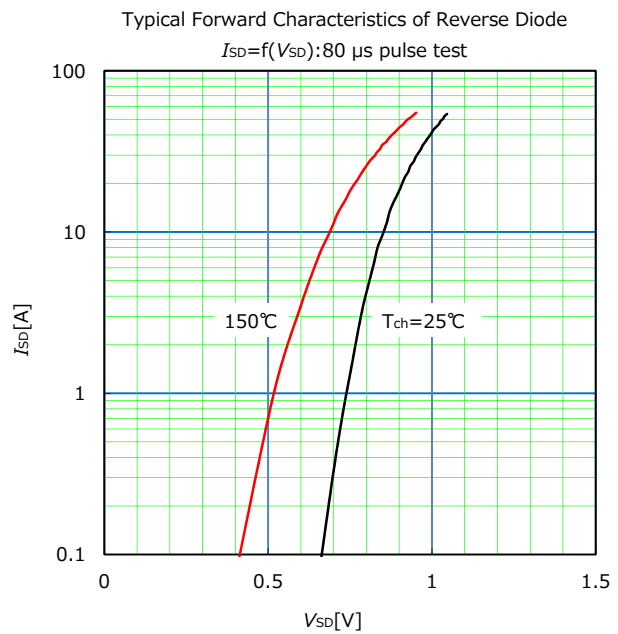
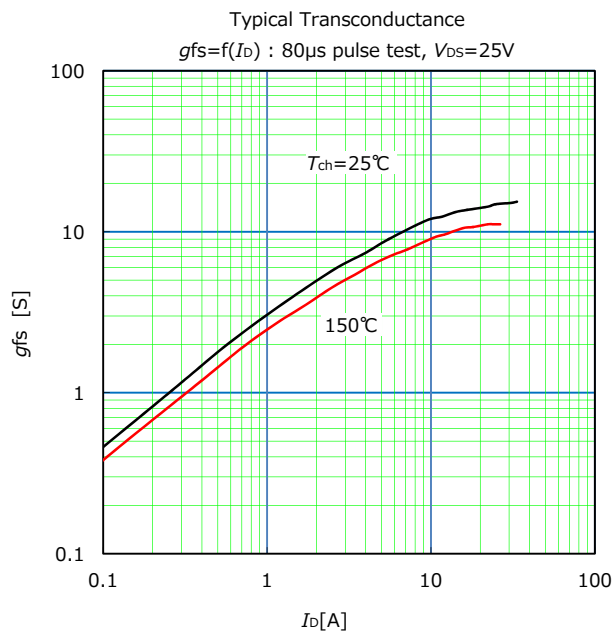
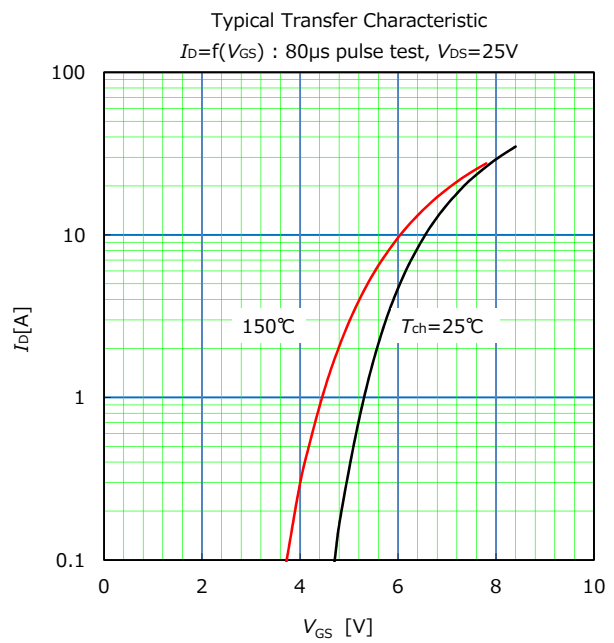
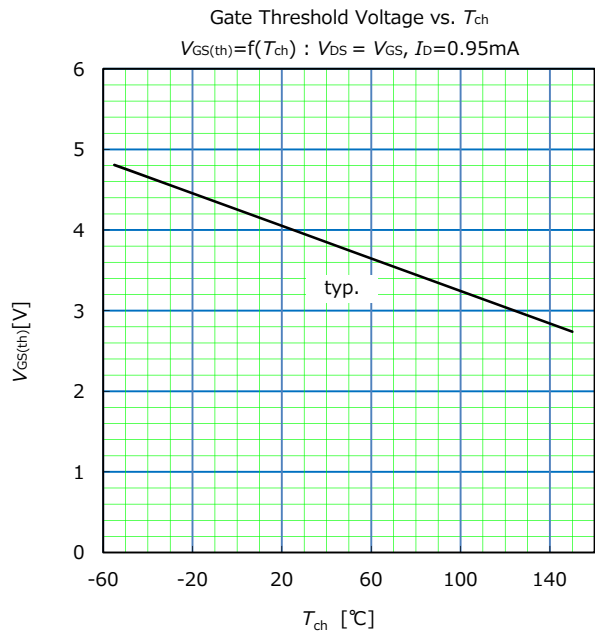
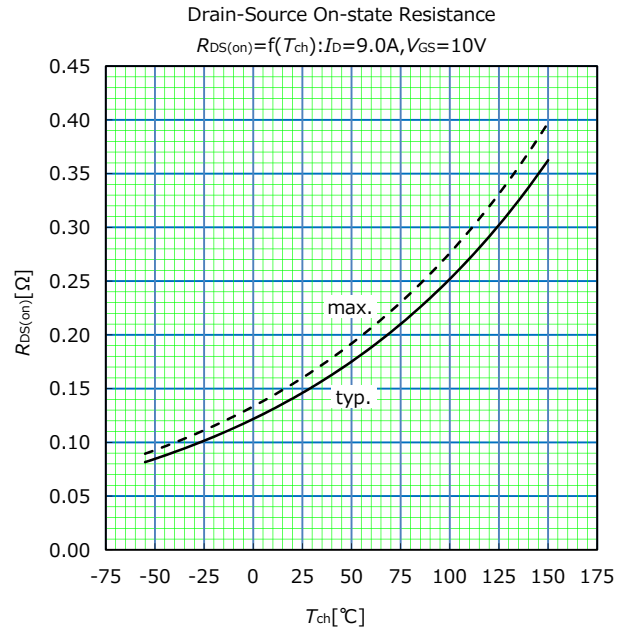
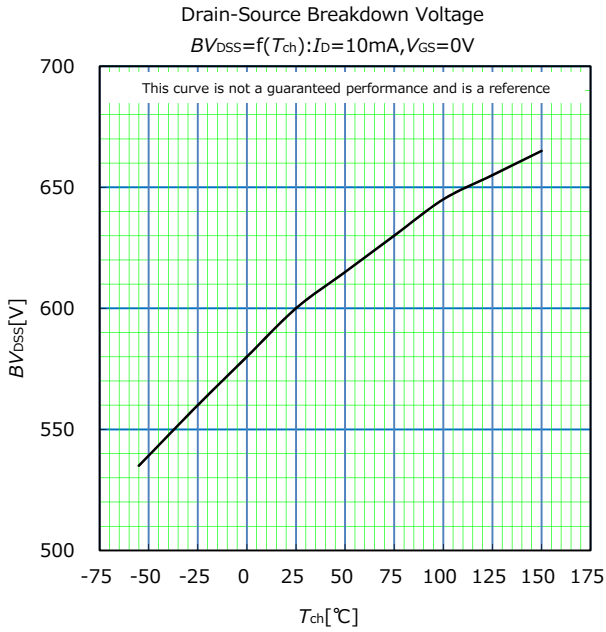
• Reverse Diode

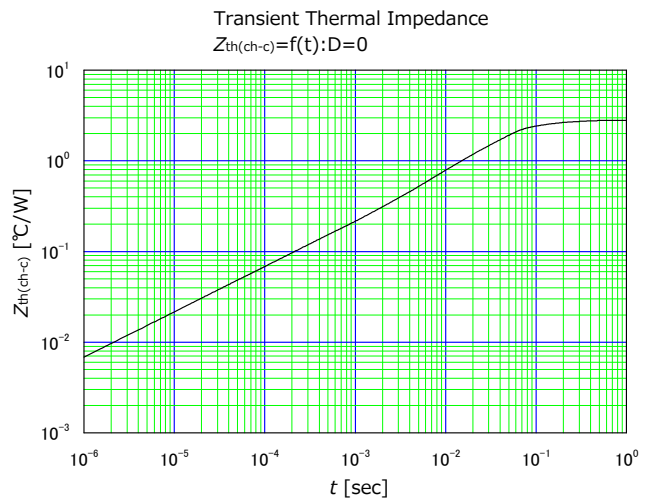
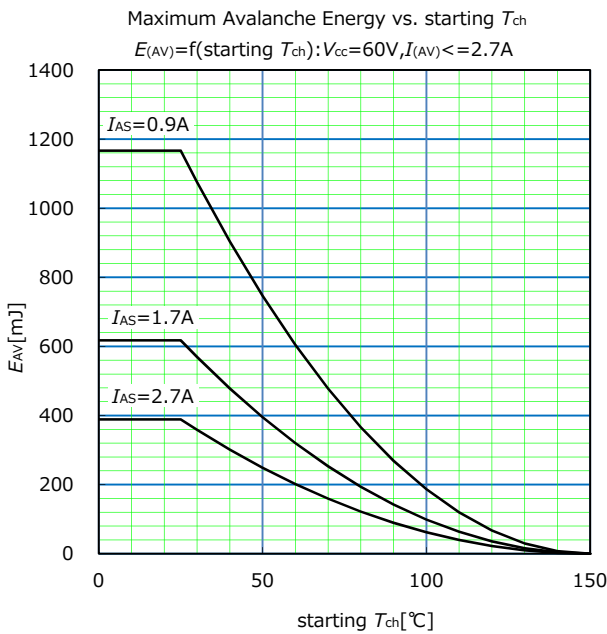
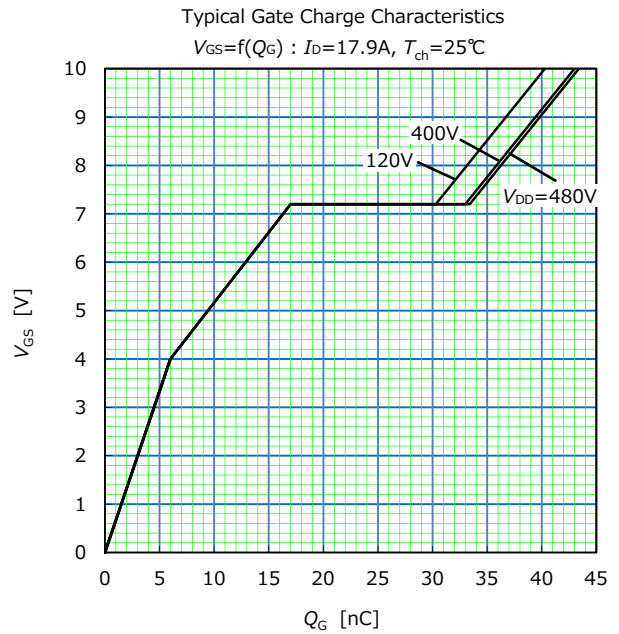
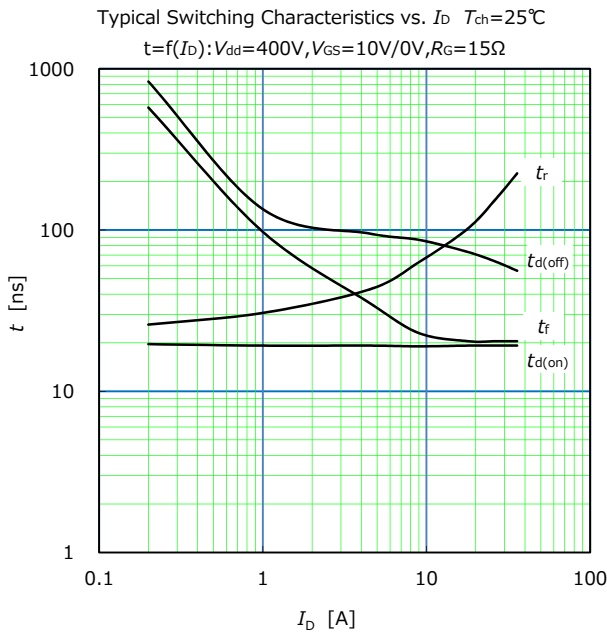
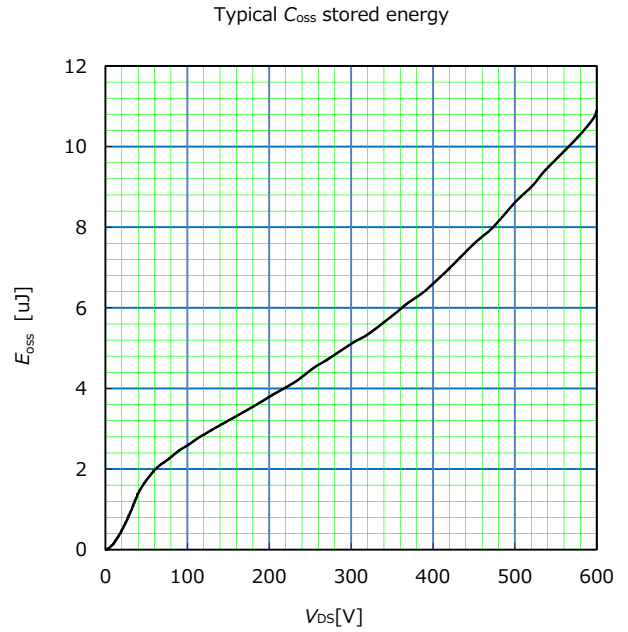
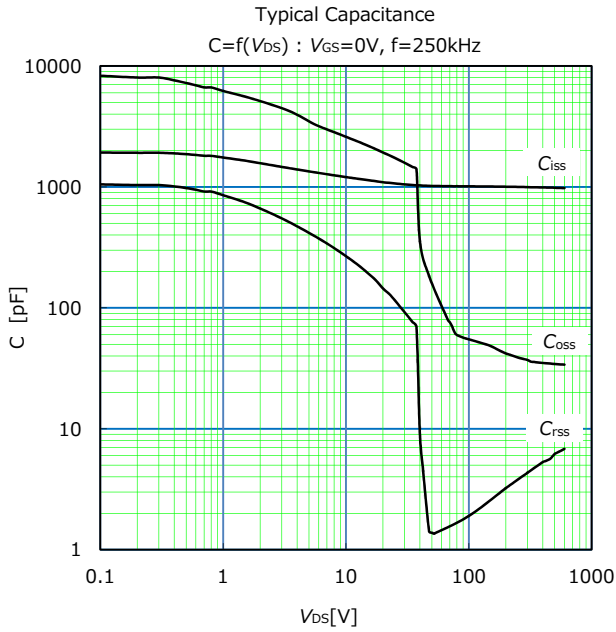
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|----------|---|------|------|------|---------|
| Diode Forward On-Voltage | V_{SD} | $I_{SD}=17.9A, V_{GS}=0V$ $T_{ch}=25^\circ\text{C}$ | - | 0.90 | 1.35 | V |
| Reverse Recovery Time | t_{rr} | $V_{DD}=400V, I_{SD}=17.9A$ -di/dt=100A/ μs $T_{ch}=25^\circ\text{C}$ See Fig.6 and Fig.7 | - | 285 | - | ns |
| Reverse Recovery Charge | Q_{rr} | | - | 3.7 | - | μC |
| Peak Reverse Recovery Current | I_{rp} | | - | 25 | - | A |

■ Thermal Resistance

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--------------------|----------------|------|------|-------|--------------------|
| Channel to Case | $R_{th(ch-c)}$ | - | - | 2.778 | $^\circ\text{C/W}$ |
| Channel to Ambient | $R_{th(ch-a)}$ | - | - | 58 | $^\circ\text{C/W}$ |







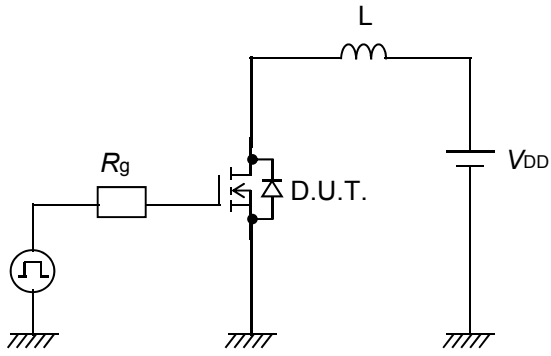


Fig.1 Avalanche Test circuit

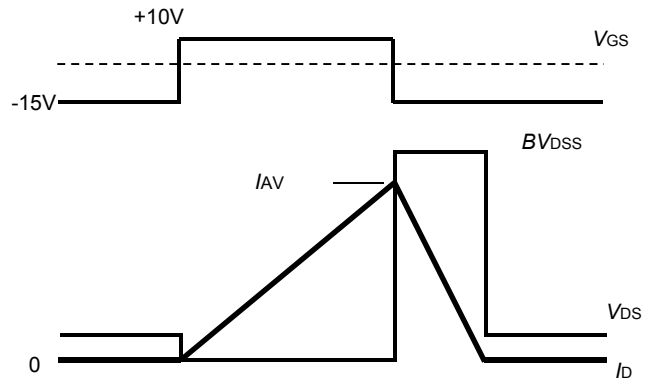


Fig.2 Operating waveforms of Avalanche Test

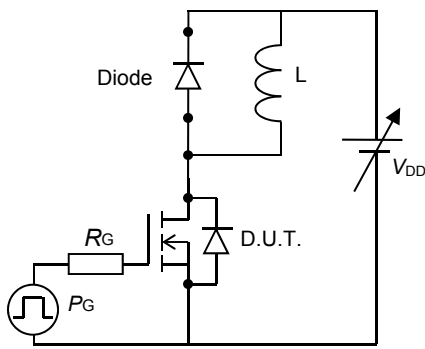


Fig.3 Switching Test circuit

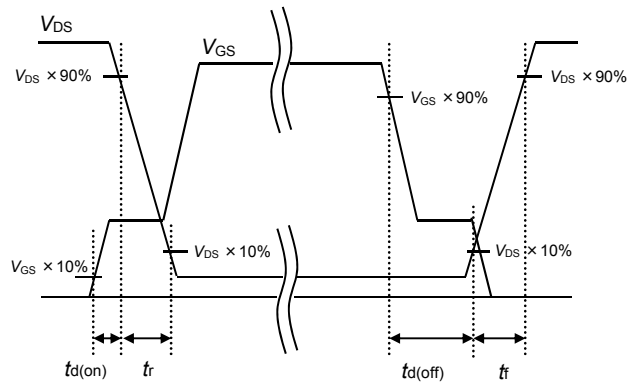


Fig.4 Operating waveform of Switching Test

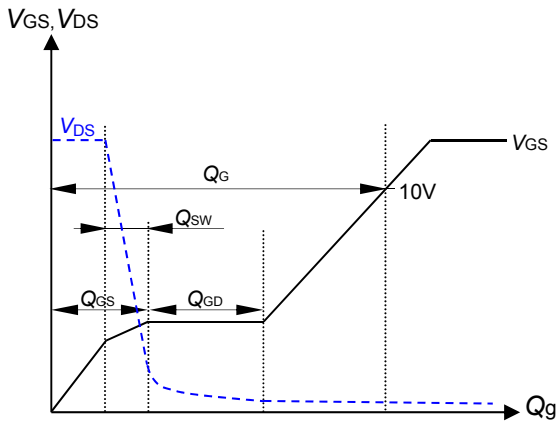


Fig.5 Operating waveform of Gate charge Test

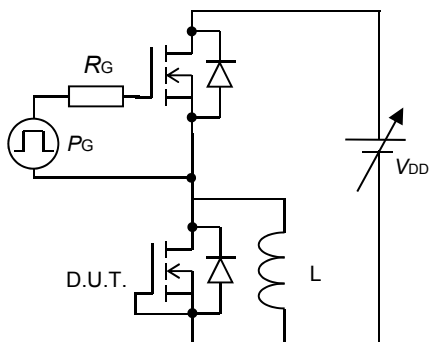


Fig.6 Reverse recovery Test circuit

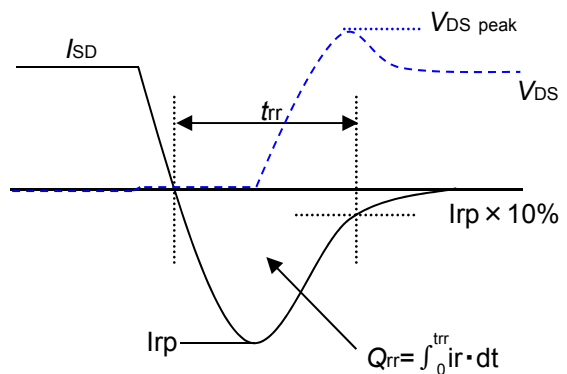
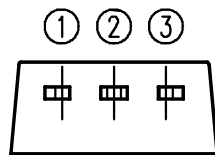
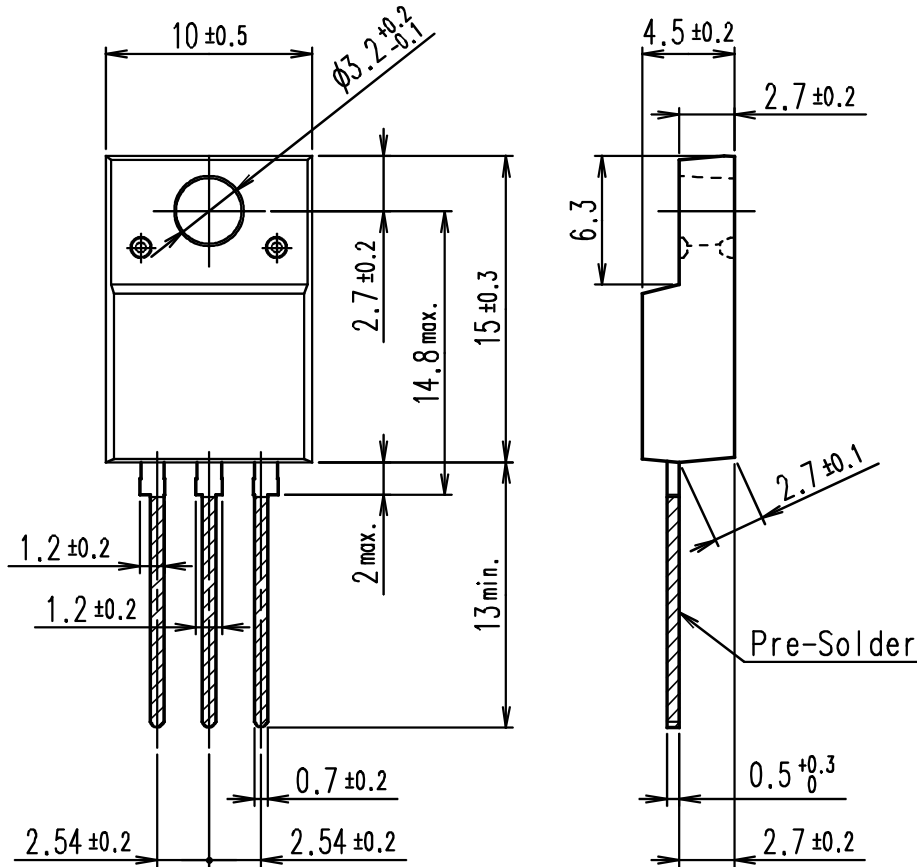


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-220F(SLS) Package

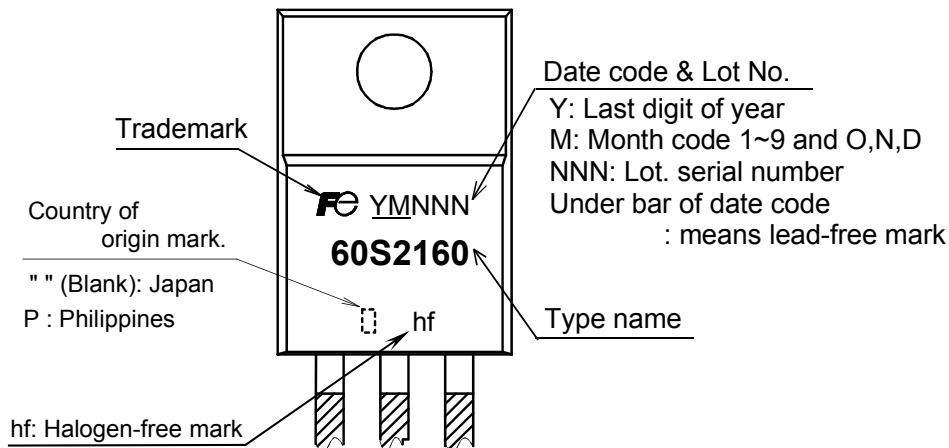


Connection

- ① Gate
- ② Drain
- ③ Source

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■ Marking



* The font (font type,size) and the trademark-size might be actually different.

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