

# FMV22N60S1

## Super J MOS<sup>®</sup> S1 series

## N-Channel enhancement mode power MOSFET

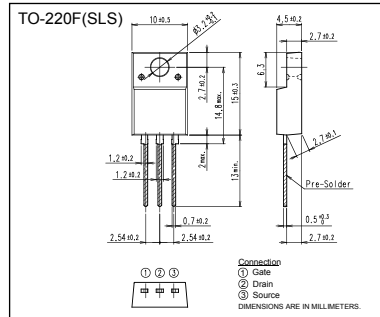
### Features

- Pb-free lead terminal
- RoHS compliant

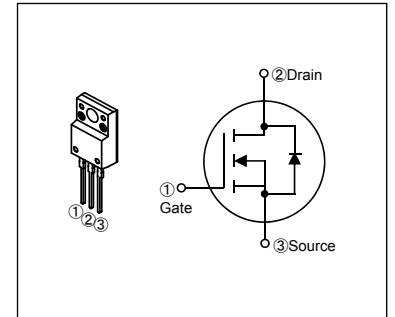
### Applications

- For switching

### Outline Drawings [mm]



### Equivalent circuit schematic



### Absolute Maximum Ratings at T<sub>c</sub>=25°C (unless otherwise specified)

Parameter	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V <sub>DS</sub>	600	V	
	V <sub>DSX</sub>	600	V	V <sub>GS</sub> =-30V
Continuous Drain Current	I <sub>D</sub>	±22	A	T <sub>c</sub> =25°C Note*1
		±14	A	T <sub>c</sub> =100°C Note*1
Pulsed Drain Current	I <sub>DP</sub>	±66	A	Note *1
Gate-Source Voltage	V <sub>GS</sub>	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I <sub>AR</sub>	6.6	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E <sub>AS</sub>	548.9	mJ	Note *3
Maximum Drain-Source dV/dt	dV <sub>DS</sub> /dt	50	kV/ns	V <sub>DS</sub> ≤ 600V
Peak Diode Recovery dV/dt	dV/dt	15	kV/ns	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note *5
Maximum Power Dissipation	P <sub>D</sub>	2.16	W	T <sub>a</sub> =25°C
		70		T <sub>c</sub> =25°C
Operating and Storage Temperature range	T <sub>ch</sub>	150	°C	
	T <sub>stg</sub>	-55 to +150	°C	
Isolation Voltage	V <sub>iso</sub>	2	kVrms	t=60sec, f=60Hz

Note \*1 : Limited by maximum channel temperature.

Note \*2 : T<sub>ch</sub> ≤ 150°C, See Fig.1 and Fig.2

Note \*3 : Starting T<sub>ch</sub> = 25°C, I<sub>AS</sub> = 4A, L = 62.9mH, V<sub>DD</sub> = 60V, R<sub>G</sub> = 50Ω, See Fig.1 and Fig.2

E<sub>AS</sub> limited by maximum channel temperature and avalanche current.

Note \*4 : I<sub>F</sub> ≤ -I<sub>D</sub>, -di/dt = 100A/μs, V<sub>DS peak</sub> ≤ 600V, T<sub>ch</sub> ≤ 150°C.

Note \*5 : I<sub>F</sub> ≤ -I<sub>D</sub>, dV/dt = 15kV/μs, V<sub>DS peak</sub> ≤ 600V, T<sub>ch</sub> ≤ 150°C.

■ Electrical Characteristics at T<sub>c</sub>=25°C (unless otherwise specified)

• Static Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA V <sub>GS</sub> =0V	600	-	-	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA V <sub>DS</sub> =V <sub>GS</sub>	2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =600V V <sub>GS</sub> =0V T <sub>ch</sub> =25°C	-	-	25	μA
		V <sub>DS</sub> =480V V <sub>GS</sub> =0V T <sub>ch</sub> =125°C	-	-	250	
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30V V <sub>DS</sub> =0V	-	10	100	nA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	I <sub>D</sub> =11A V <sub>GS</sub> =10V	-	0.136	0.16	Ω
Gate resistance	R <sub>G</sub>	f=1MHz, open drain	-	3.5	-	Ω

• Dynamic Ratings

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g <sub>fs</sub>	I <sub>D</sub> =11A V <sub>DS</sub> =25V	10.5	21	-	S
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V	-	1710	-	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> =0V	-	3660	-	
Reverse Transfer Capacitance	C <sub>rss</sub>	f=1MHz	-	350	-	
Effective output capacitance, energy related (Note *6)	C <sub>o(er)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0...480V	-	100	-	
Effective output capacitance, time related (Note *7)	C <sub>o(tr)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0...480V I <sub>D</sub> =constant	-	350	-	
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =10V I <sub>D</sub> =11A, R <sub>G</sub> =20Ω	-	52	-	ns
Turn-Off Time	t <sub>d(off)</sub>	See Fig.3 and Fig.4	-	18.5	-	
	t <sub>f</sub>		-	146	-	
Total Gate Charge	Q <sub>G</sub>		-	17.5	-	nC
Gate-Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> =480V, I <sub>D</sub> =22A V <sub>GS</sub> =10V	-	57	-	
Gate-Drain Charge	Q <sub>GD</sub>	See Fig.5	-	14	-	
Drain-Source crossover Charge	Q <sub>SW</sub>		-	19.5	-	

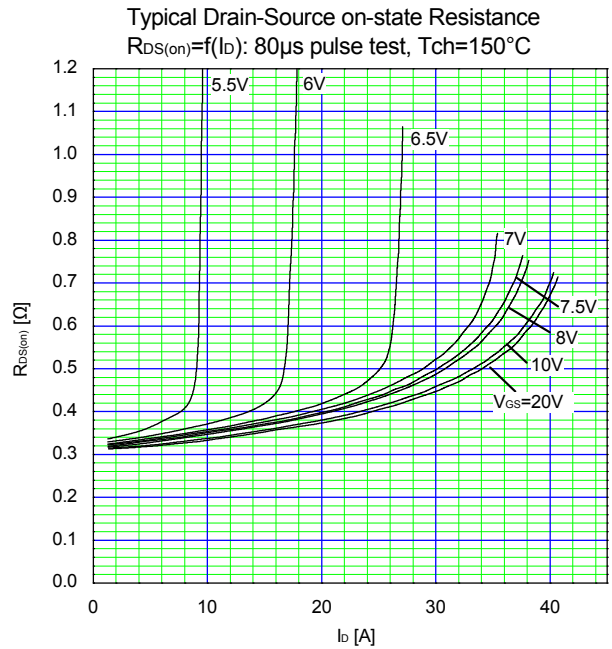
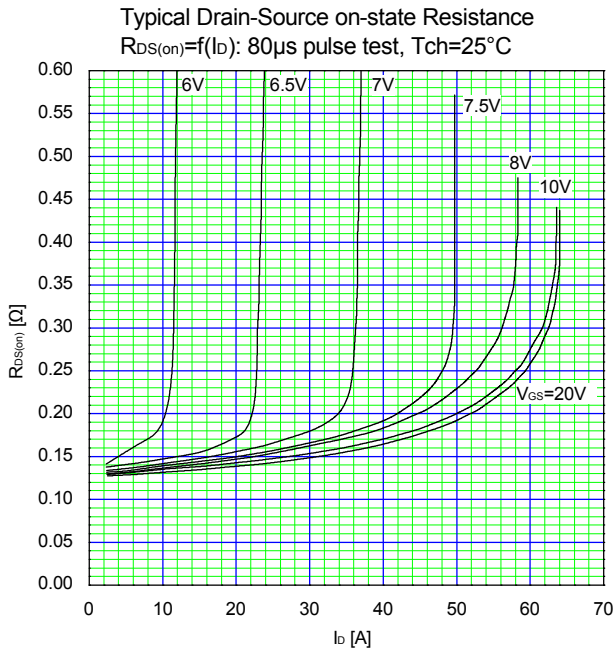
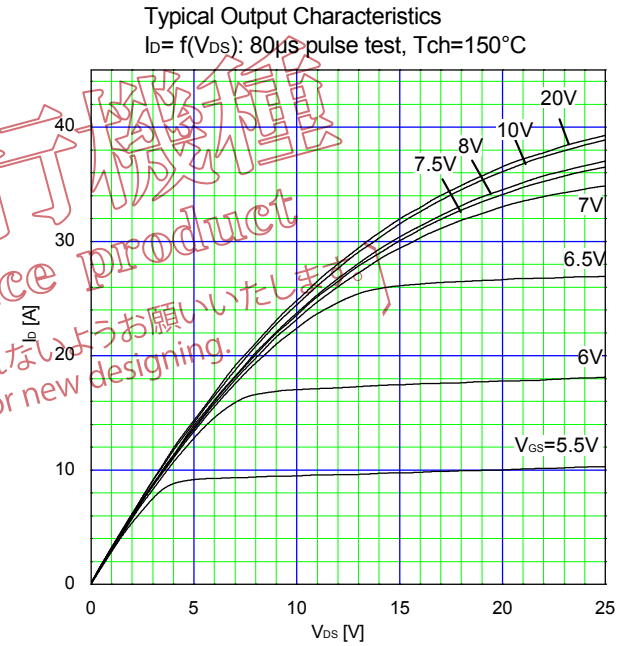
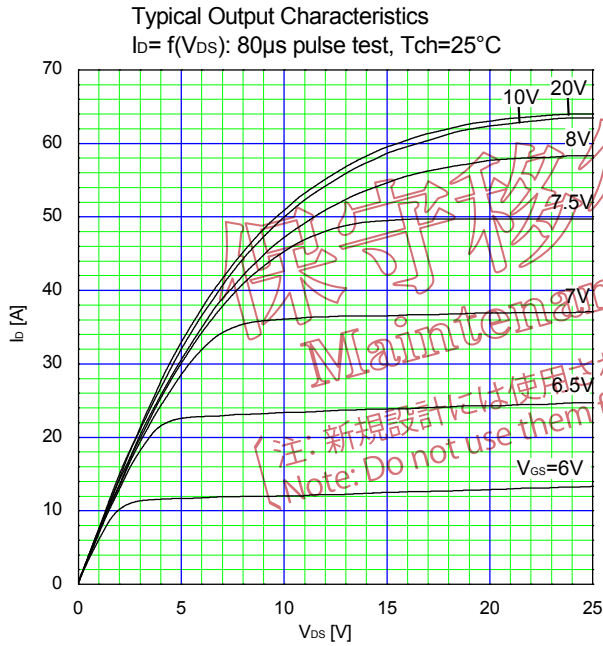
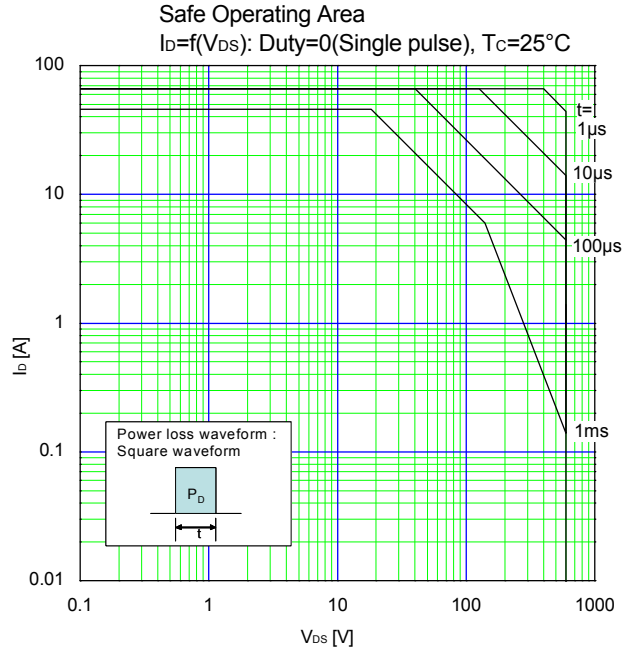
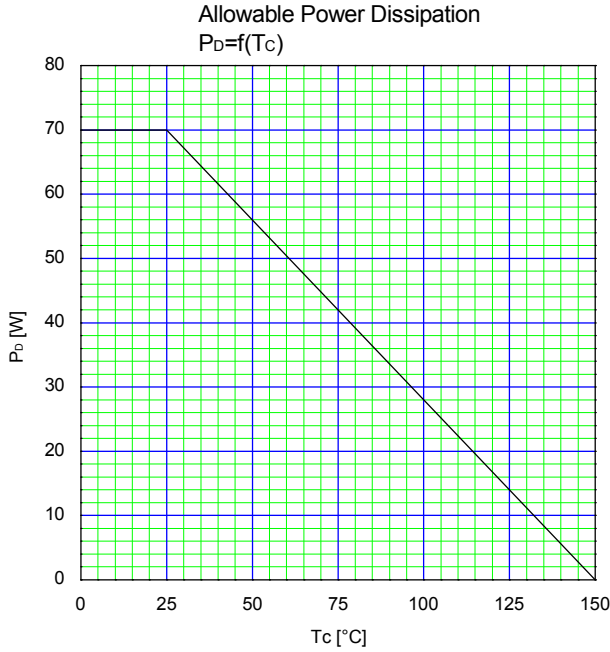
Note \*6 : C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% BV<sub>DSS</sub>.  
 Note \*7 : C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging times as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% BV<sub>DSS</sub>.

• Reverse Diode

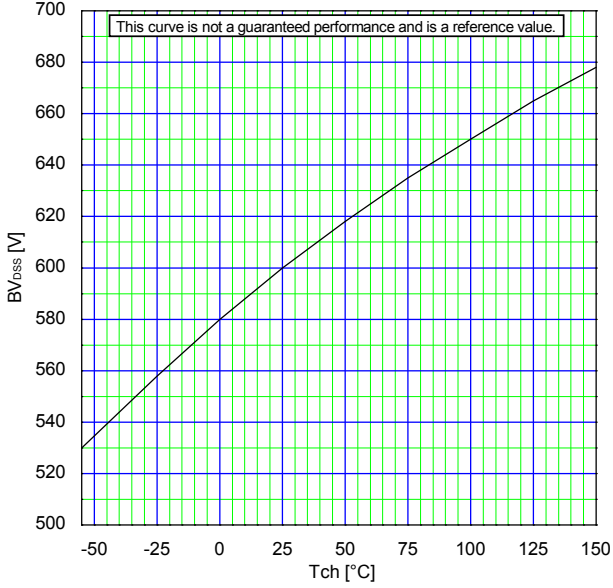
Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	I <sub>AV</sub>	L=14mH, T <sub>ch</sub> =25°C See Fig.1 and Fig.2	6.6	-	-	V
Diode Forward On-Voltage	V <sub>SD</sub>	I <sub>F</sub> =22A, V <sub>GS</sub> =0V T <sub>ch</sub> =25°C	-	0.9	1.35	V
Reverse Recovery Time	t <sub>rr</sub>		-	380	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =22A, V <sub>DD</sub> =400V -di/dt=100A/μs T <sub>ch</sub> =25°C See Fig.6 and Fig.7	-	6.5	-	μC
Peak Reverse Recovery Current	I <sub>rp</sub>		-	34	-	A

■ Thermal Resistance

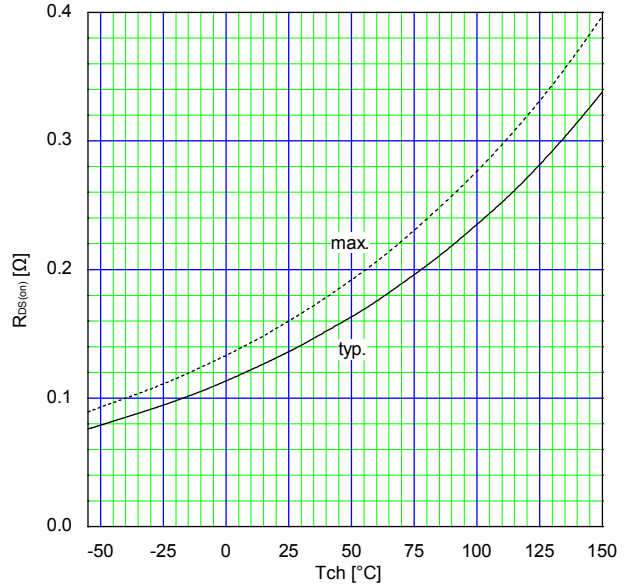
Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	R <sub>th(ch-c)</sub>	-	-	1.79	°C/W
Channel to Ambient	R <sub>th(ch-a)</sub>	-	-	58	°C/W



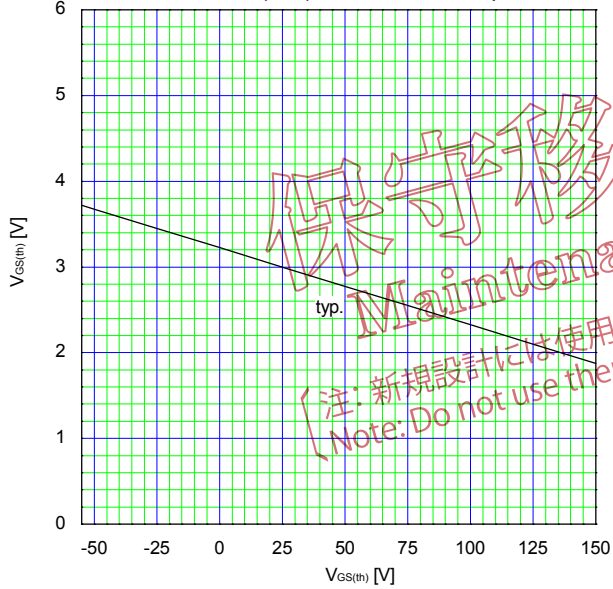
Drain-Source Breakdown Voltage  
 $BV_{DSS}=f(T_{ch}): I_D=10mA, V_{GS}=0V$



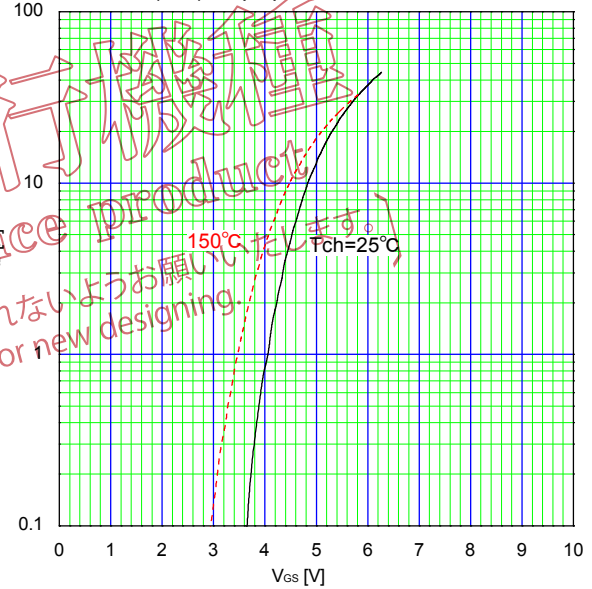
Drain-Source On-state Resistance  
 $R_{DS(on)}=f(T_{ch}): I_D=11A, V_{GS}=10V$



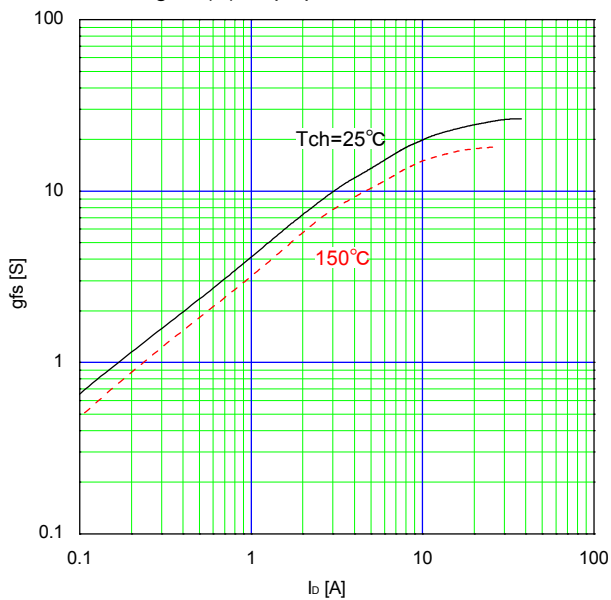
Gate Threshold Voltage vs. T<sub>ch</sub>  
 $V_{GS(th)}=f(T_{ch}): V_{DS}=V_{GS}, I_D=250\mu A$



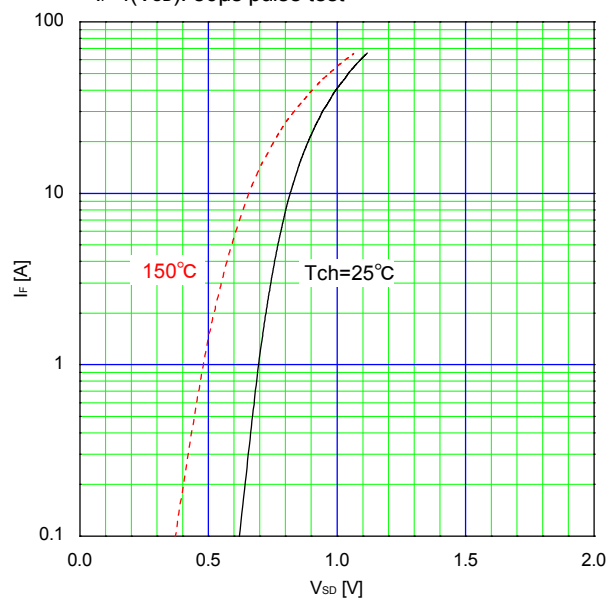
Typical Transfer Characteristic  
 $I_D=f(V_{GS}): 80\mu s \text{ pulse test}, V_{DS}=25V$



Typical Transconductance  
 $g_{fs}=f(I_D): 80\mu s \text{ pulse test}, V_{DS}=25V$

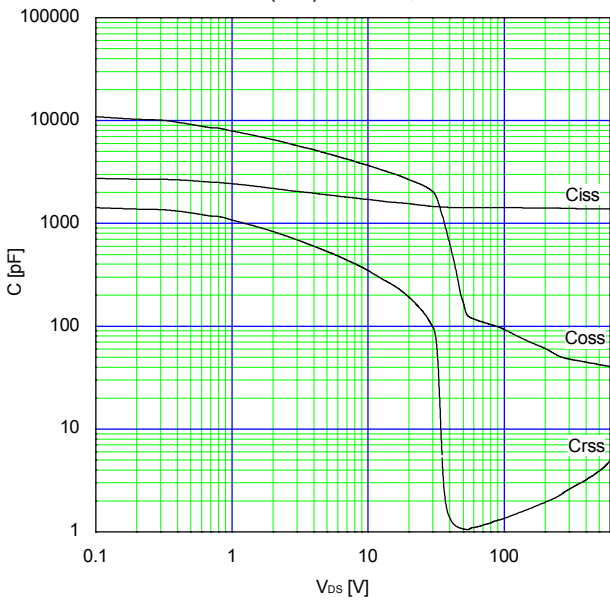


Typical Forward Characteristics of Reverse Diode  
 $I_F=f(V_{SD}): 80\mu s \text{ pulse test}$

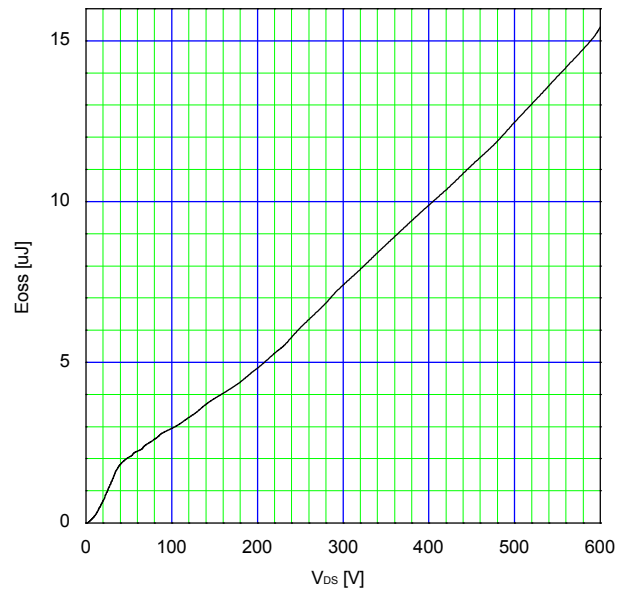


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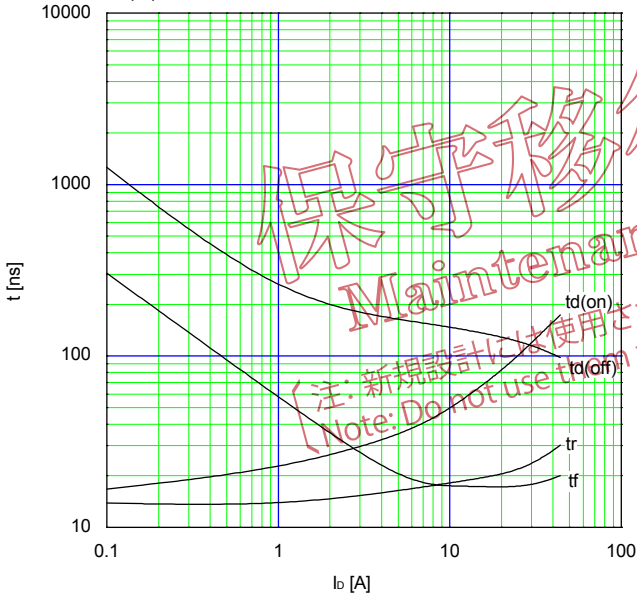
Typical Capacitance  
 $C=f(V_{DS}): V_{GS}=0V, f=1MHz$



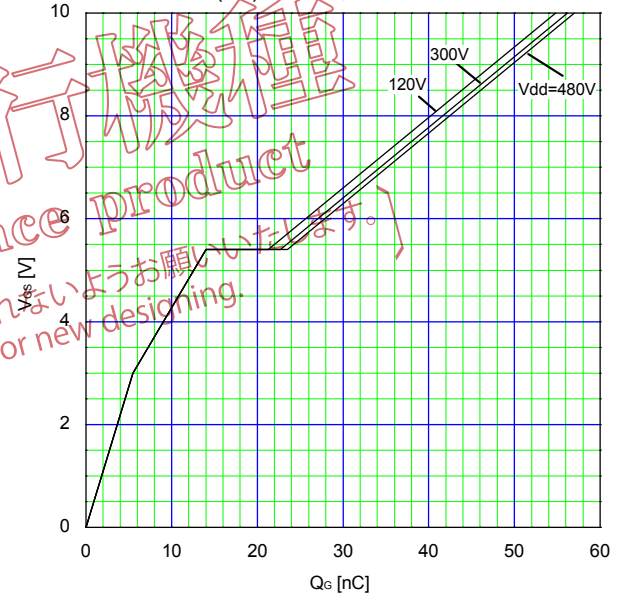
Typical  $C_{oss}$  stored energy



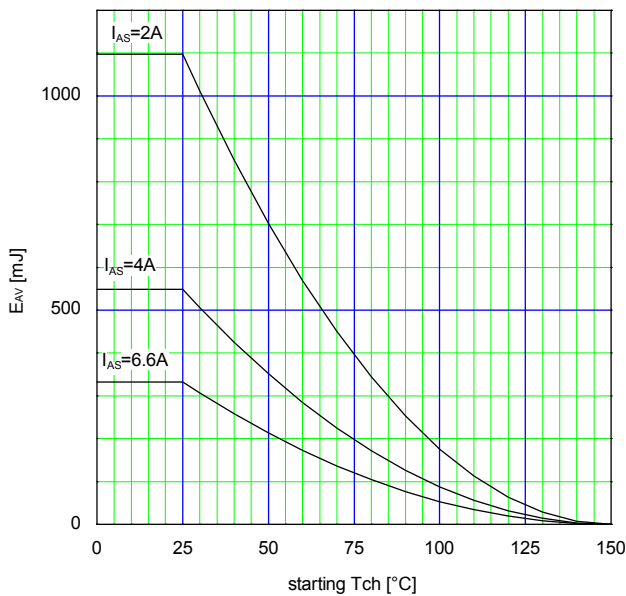
Typical Switching Characteristics vs.  $I_D$   $T_{ch}=25^\circ C$   
 $t=f(I_D): V_{dd}=400V, V_{GS}=10V/0V, R_G=20\Omega$



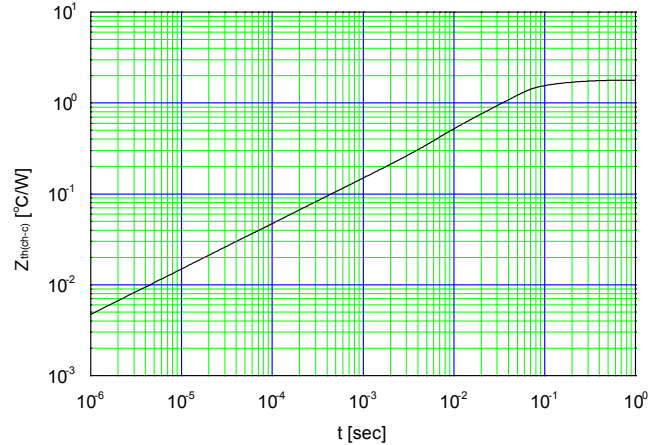
Typical Gate Charge Characteristics  
 $V_{GS}=f(Q_G): I_D=22A, T_{ch}=25^\circ C$



Maximum Avalanche Energy vs. starting  $T_{ch}$   
 $E_{AV}=f(\text{starting } T_{ch}): V_{CC}=60V, I_{AV}<=6.6A$



Transient Thermal Impedance  
 $Z_{th(ch-c)}=f(t): D=0$



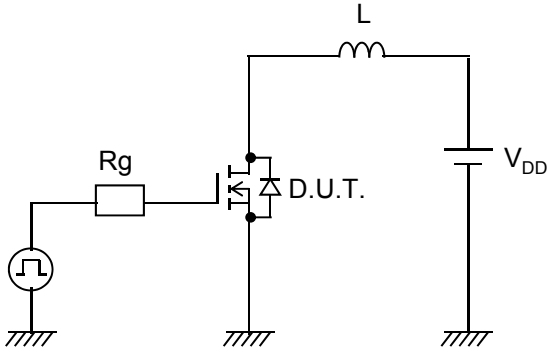


Fig.1 Avalanche Test circuit

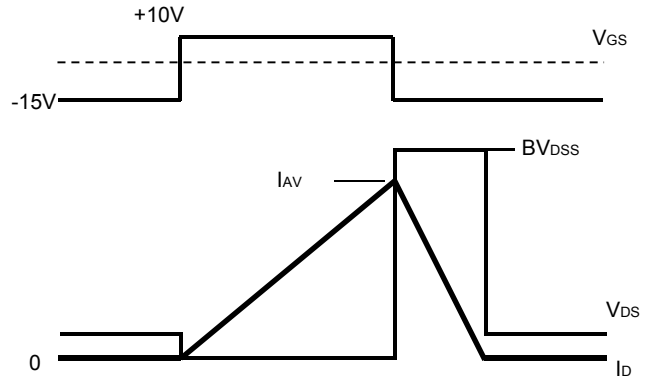


Fig.2 Operating waveforms of Avalanche Test

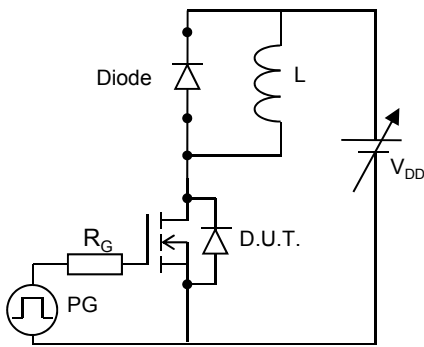


Fig.3 Switching Test circuit

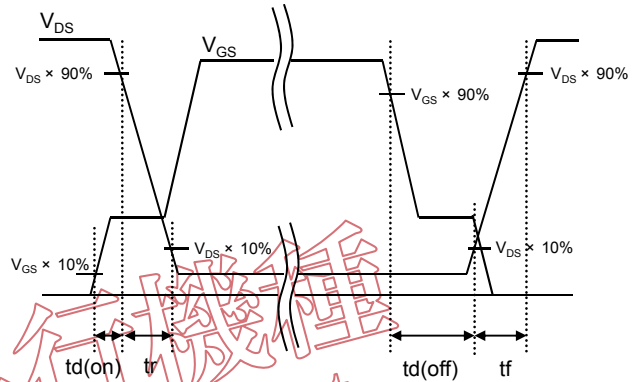


Fig.4 Operating waveform of Switching Test

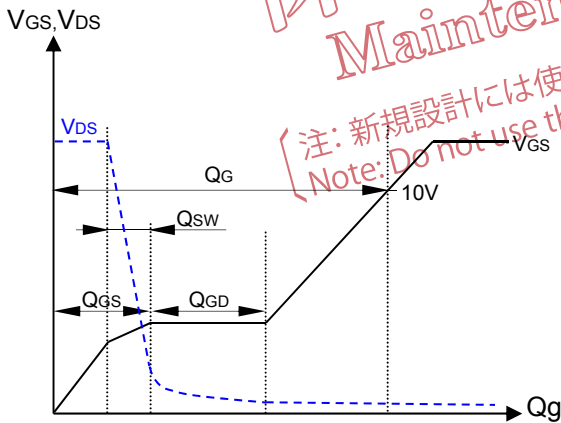


Fig.5 Operating waveform of Gate charge Test

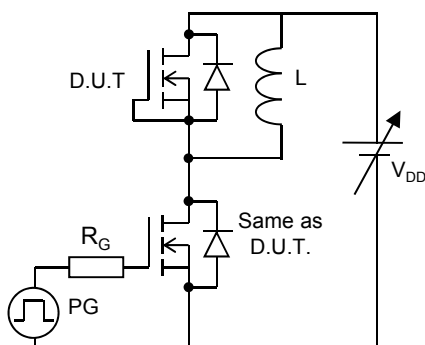


Fig.6 Reverse recovery Test circuit

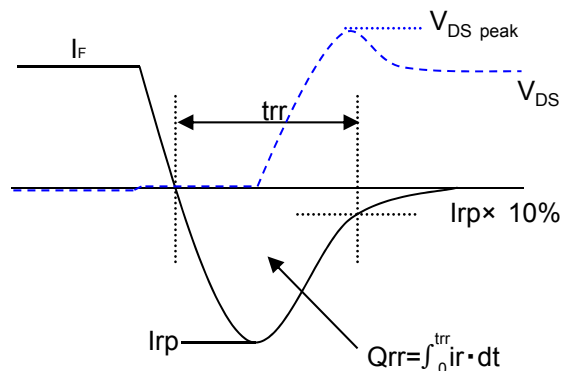
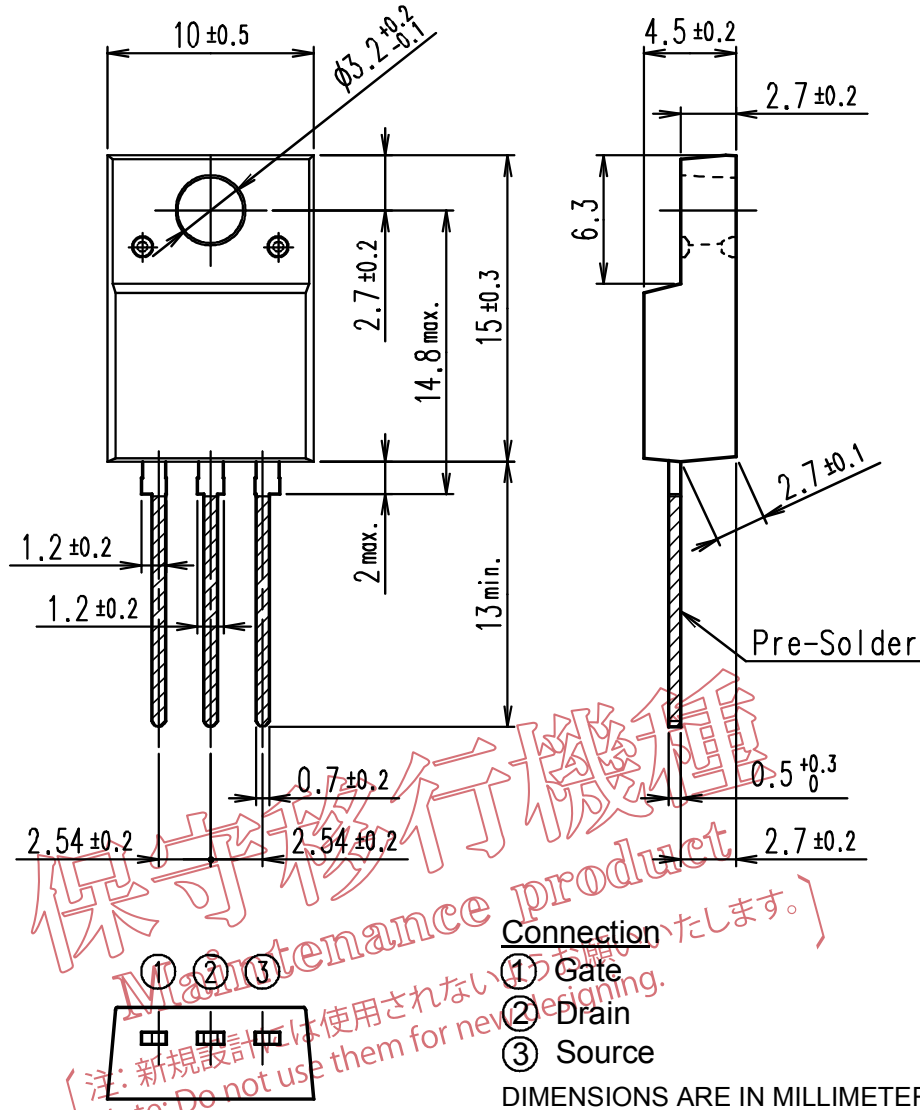


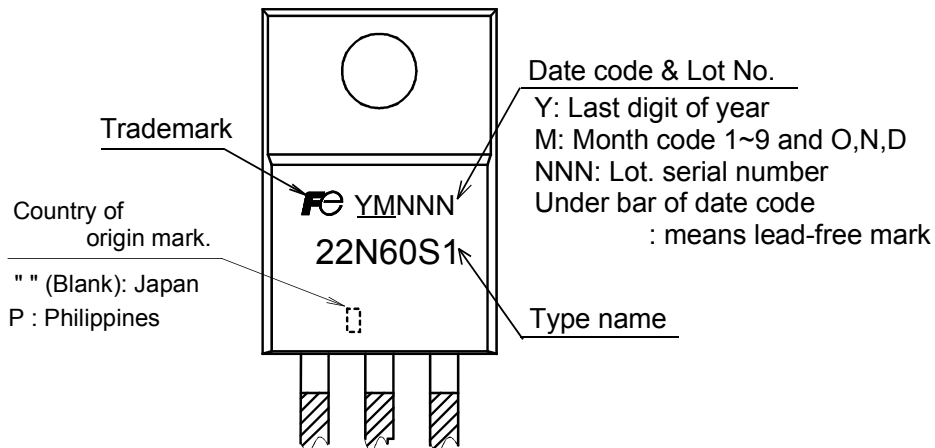
Fig.7 Operating waveform of Reverse recovery Test

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■ Outview: TO-220F(SLS) Package



■ Marking



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