OptiMOS®2 Power-Transistor

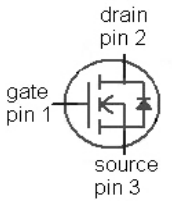
Features

- N-channel, logic level
- Excellent gate charge x ☎DS(on) product (FOM)
- Very low on-resistance ☎DS(on)
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Ideal for high-frequency switching and synchronous rectification

Product Summary

DS	100	V
DS(on),max	5.1	mΩ
D	100	A

Type	IPP05CN10L G
	
Package	PG-TO220-3
Marking	05CN10L



Maximum ratings, at ℐj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	D	ℐC=25 °C[2]	100	A
		ℐC=100 °C	100	
Pulsed drain current[3]	D,pulse	ℐC=25 °C	400	
Avalanche energy, single pulse	AS	D=100 A, ☎GS=25 Ω	826	mJ
Reverse diode d /d	d /d	D=100 A, DS=80 V, d /d =100 A/µs, j,max=175 °C	6	kV/µs
Gate source voltage [4]	GS		±20	V
Power dissipation	tot	C=25 °C	300	W
Operating and storage temperature	j, stg		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm² cooling area[5]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250 µA	1.2	1.85	2.4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	4.8	6.4	mΩ
		V_{GS}=10 V, I_D=100 A	-	4.2	5.1	
Gate resistance	R_G		-	1.8	-	Ω
Transconductance	g_{fs}	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=100 A	106	212	-	S

[1] J-STD20 and JESD22

[2] Current is limited by bondwire; with an R_{thJC}=0.5 K/W the chip is able to carry 161 A.

[3] See figure 3

[4] T_{jmax}=150 °C and duty cycle D=0.01 for V_{gs}<-5V

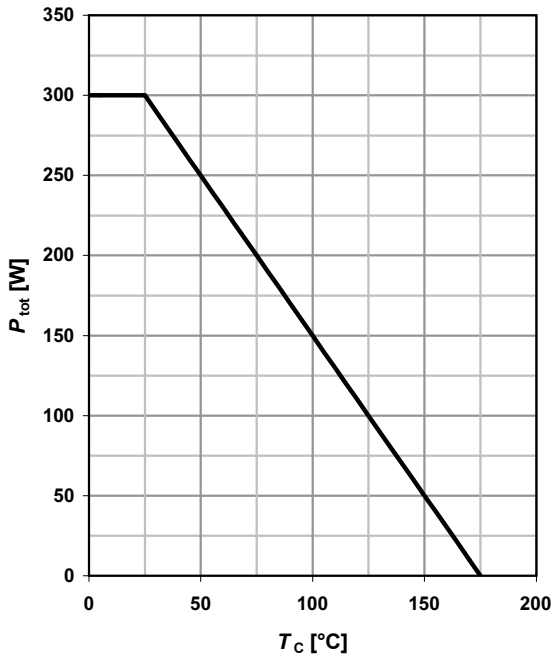
[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	11700	15600	pF
Output capacitance	C_{oss}		-	1480	1970	
Reverse transfer capacitance	C_{rss}		-	75	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50 V, V_{GS}=4.5 V, I_D=100 A, R_G=1.6 Ω	-	46	-	ns
Rise time	t_r		-	288	-	
Turn-off delay time	$t_{d(off)}$		-	62	-	
Fall time	t_f		-	37	-	
Gate Charge Characteristics[6]						
Gate to source charge	Q_{gs}	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V	-	40	-	nC
Gate to drain charge	Q_{gd}		-	27	-	
Switching charge	Q_{sw}		-	31	-	
Gate charge total	Q_g		-	163	-	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V
Output charge	Q_{oss}	V_{DD}=50 V, V_{GS}=0 V	-	152	-	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	100	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.97	1.2	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=I_S, dI_F/dt =100 A/µs	-	106		ns
Reverse recovery charge	Q_{rr}		-	285	-	nC

[6] See figure 16 for gate charge parameter definition

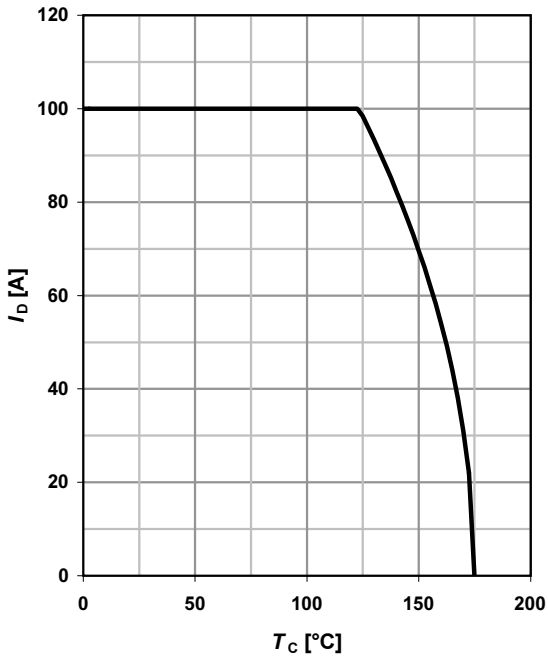
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

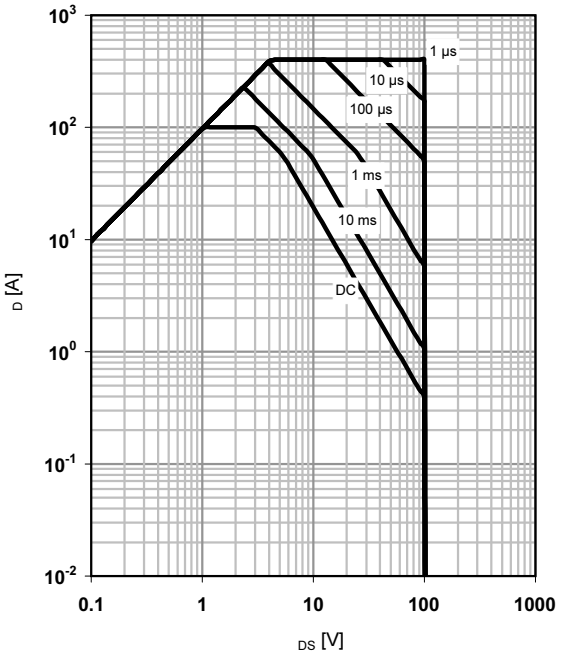
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $\Omega=0$

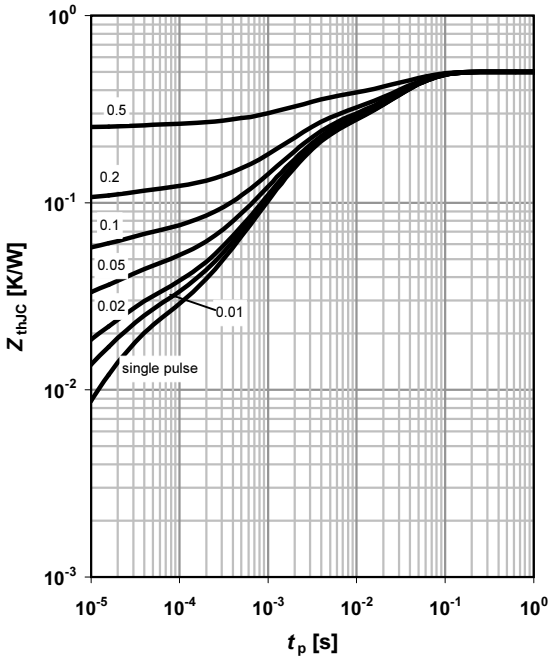
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

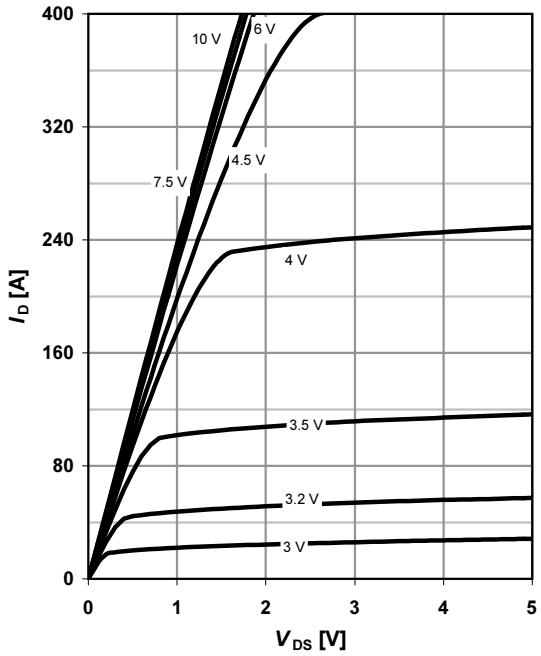
parameter: $\Omega=t_p/T$



5 Typ. output characteristics

$_D$=f($_{DS}$); $_j$=25 °C

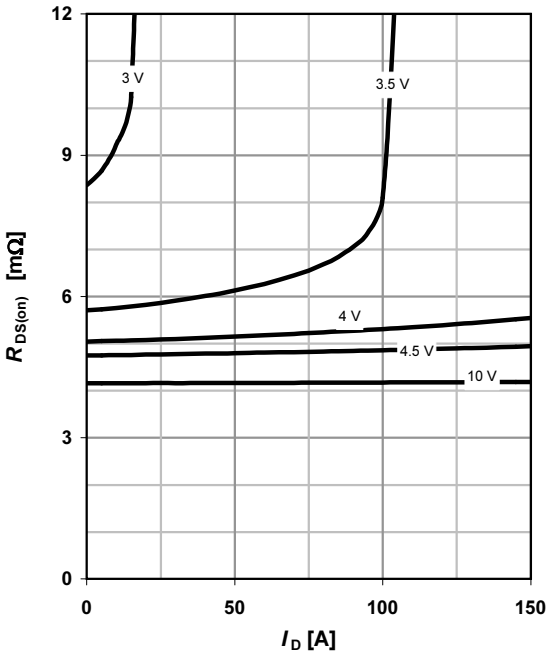
parameter: $_{GS}$



6 Typ. drain-source on resistance

$_{DS(on)}$=f($_D$); $_j$=25 °C

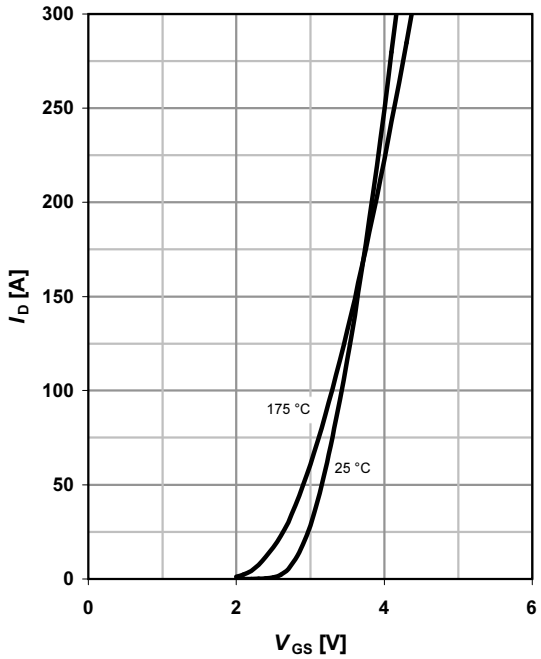
parameter: $_{GS}$



7 Typ. transfer characteristics

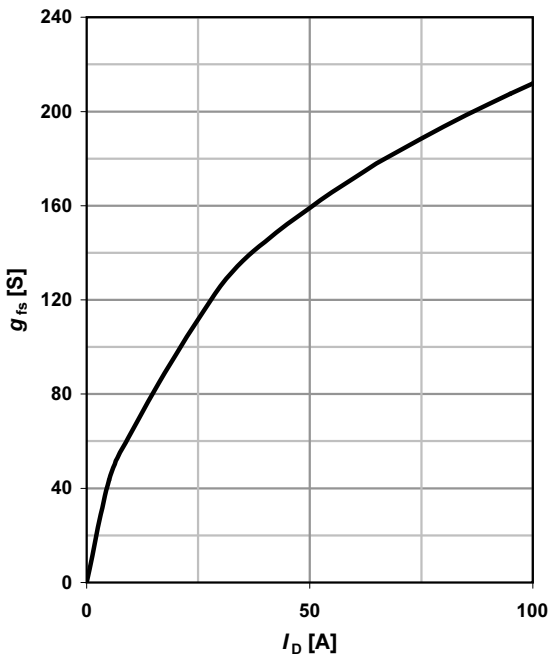
$_D$=f($_{GS}$); | $_{DS}$|>2| $_D$| $_{DS(on)max}$

parameter: $_j$



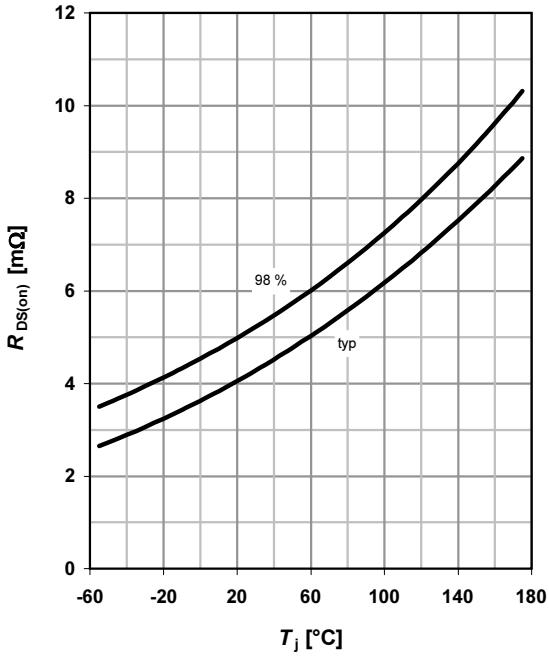
8 Typ. forward transconductance

$_{fs}$=f($_D$); $_j$=25 °C



9 Drain-source on-state resistance

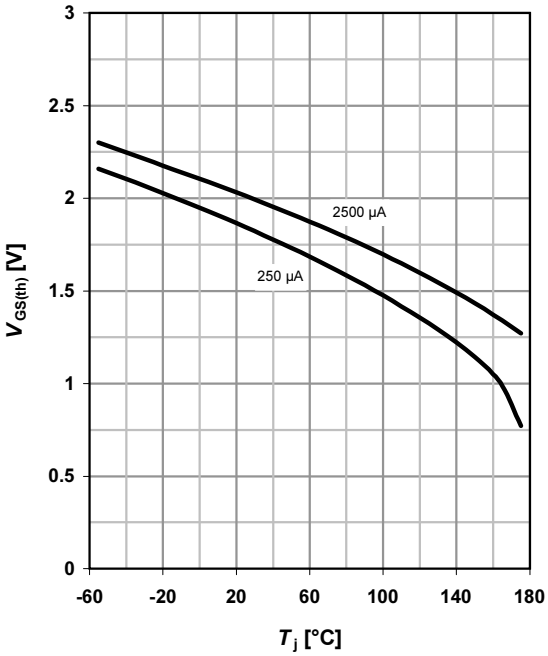
$R_{DS(on)}=f(T_j)$; $I_D=100$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

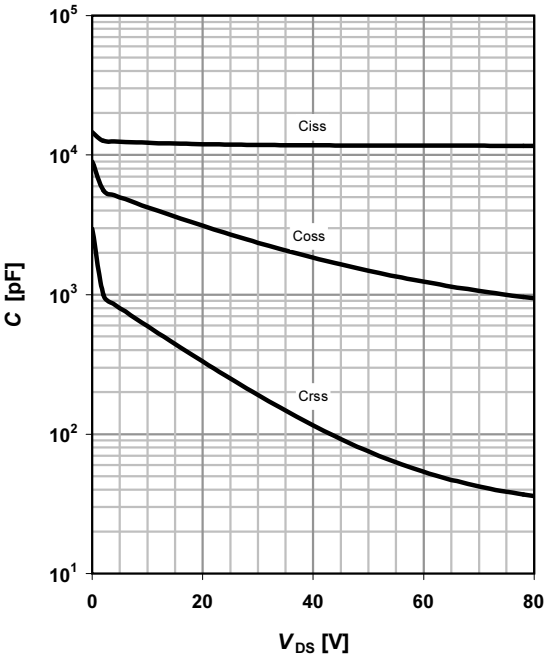
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

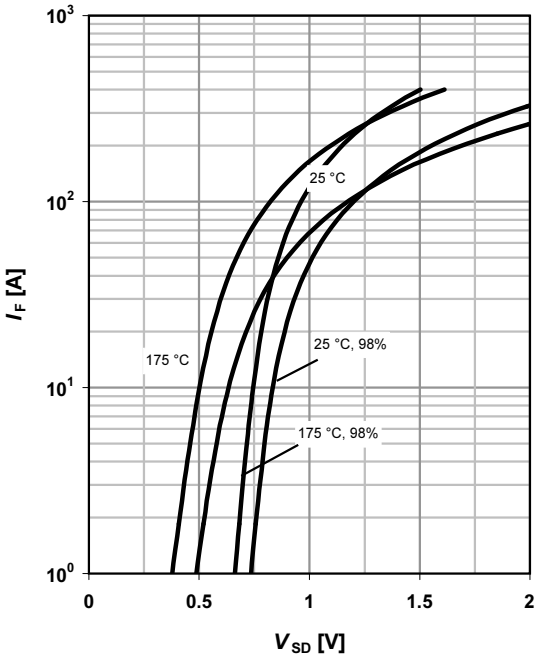
□ =f(DS); GS=0 V; =1 MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

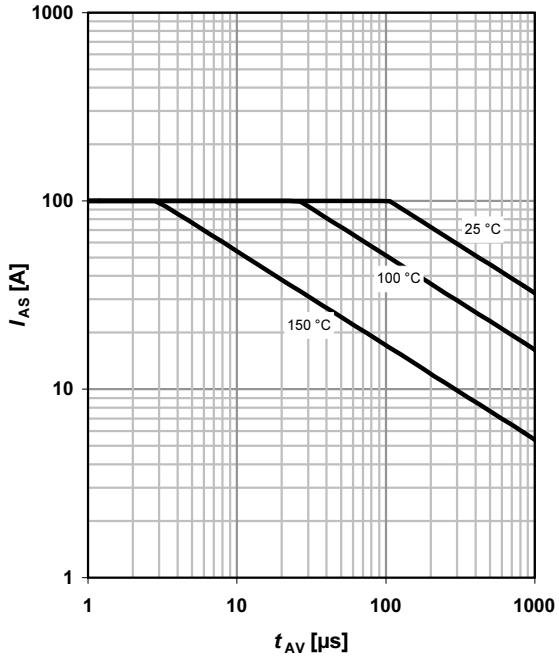
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$

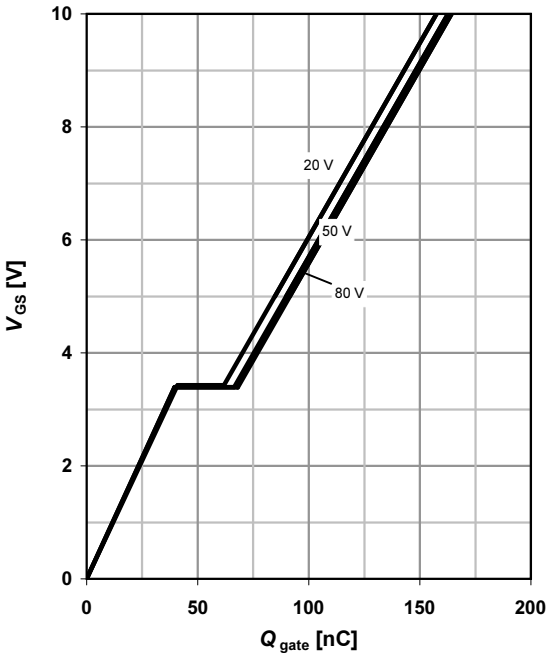
parameter: $T_{j(start)}$



14 Typ. gate charge

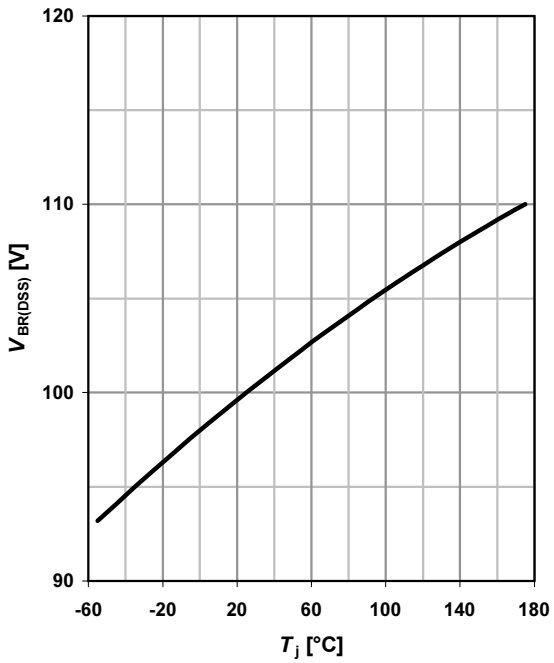
$V_{GS}=f(Q_{gate})$; $I_D=100$ A pulsed

parameter: V_{DD}

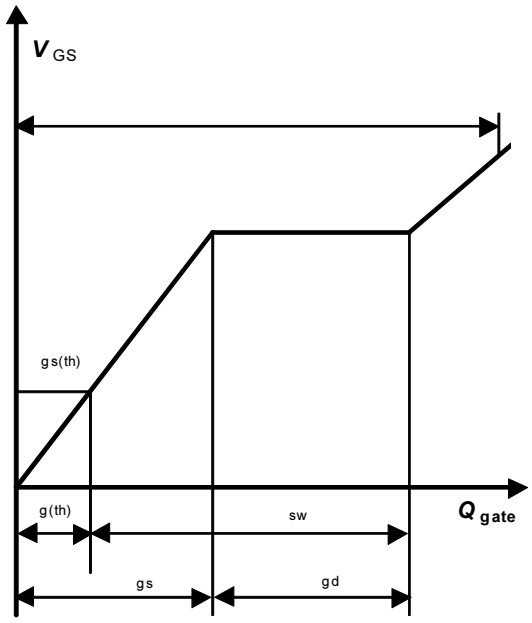


15 Drain-source breakdown voltage

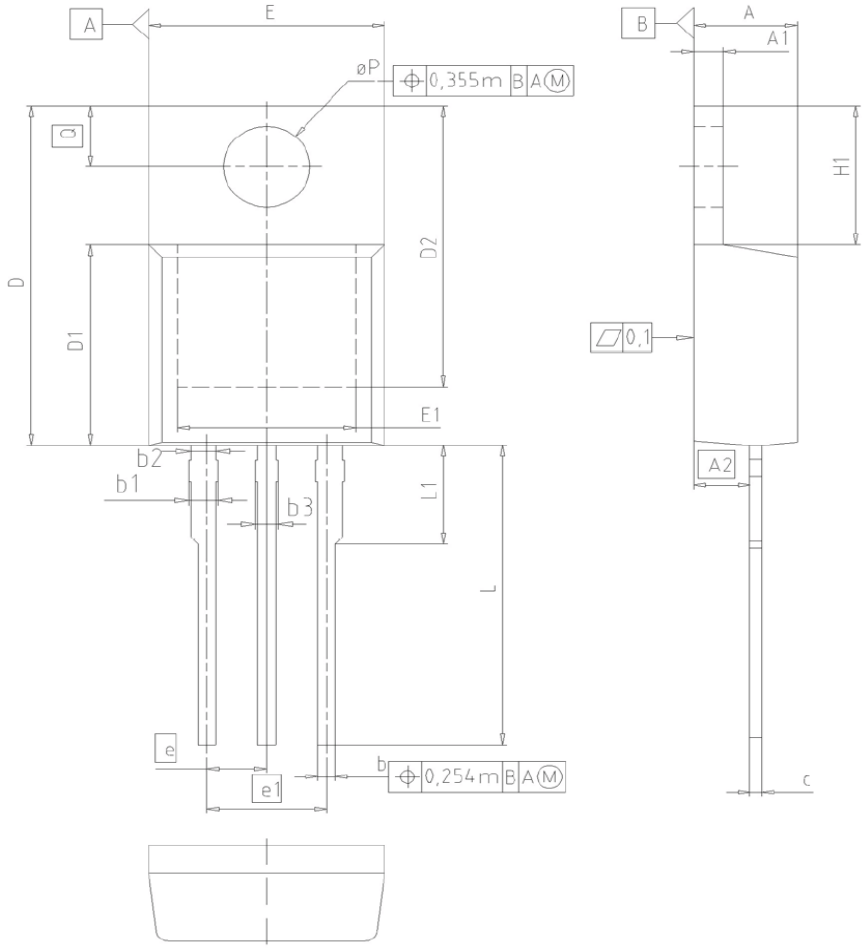
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA



16 Gate charge waveforms



PG-TO220-3: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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